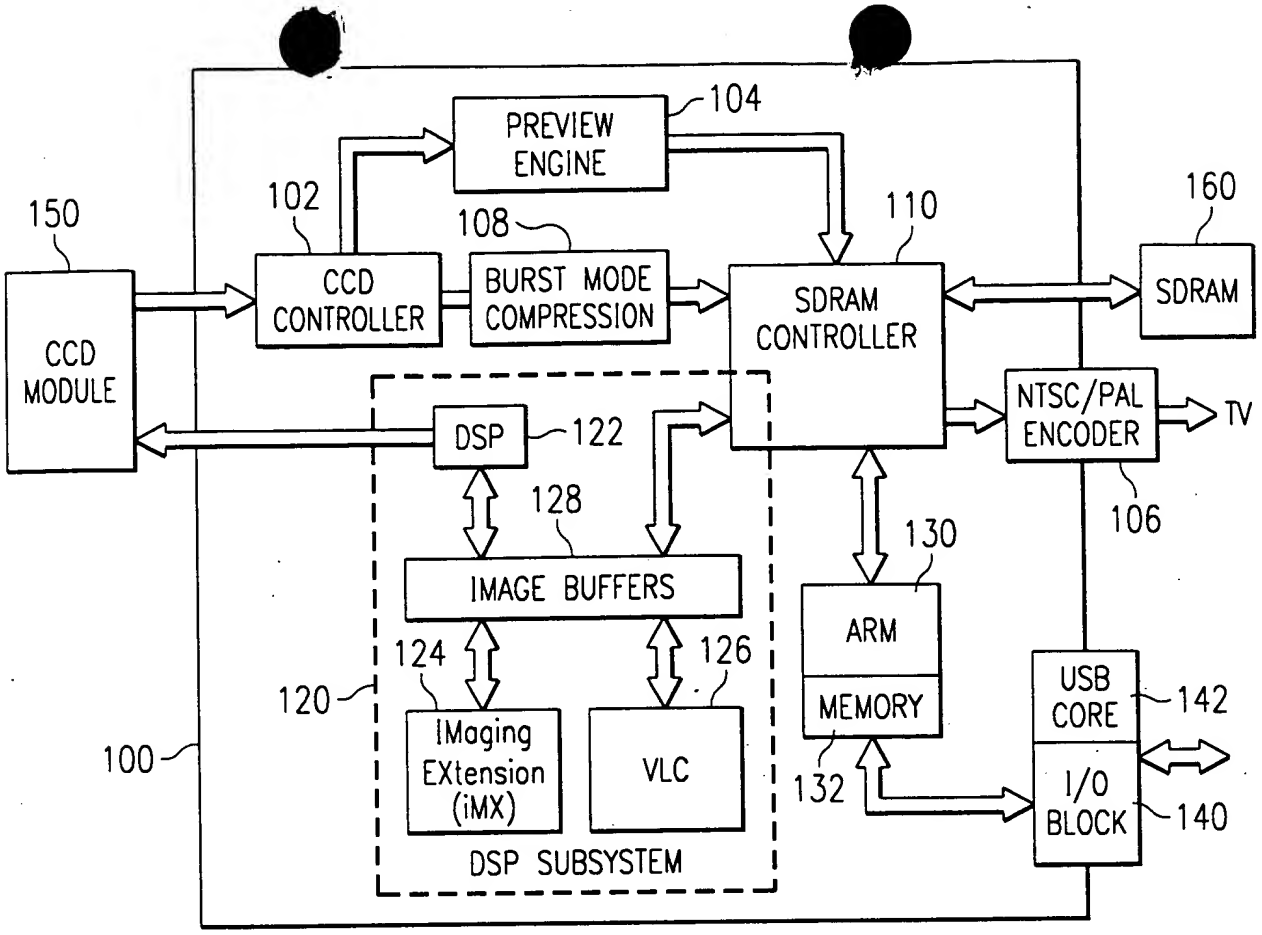

PREVIEW ENGINE
104
102
108
110
160
150
CCD CONTROLLER
BURST MODE COMPRESSION
SDRAM CONTROLLER
SDRAM
CCD MODULE
NTSC/PAL ENCODER
TV
DSP
122
128
106
130
IMAGE BUFFERS
ARM
MEMORY
124
126
USB CORE
142
120
IMaging EXtension (iMX)
VLC
I/O BLOCK
140
100
132
DSP SUBSYSTEM

FIG. 1a

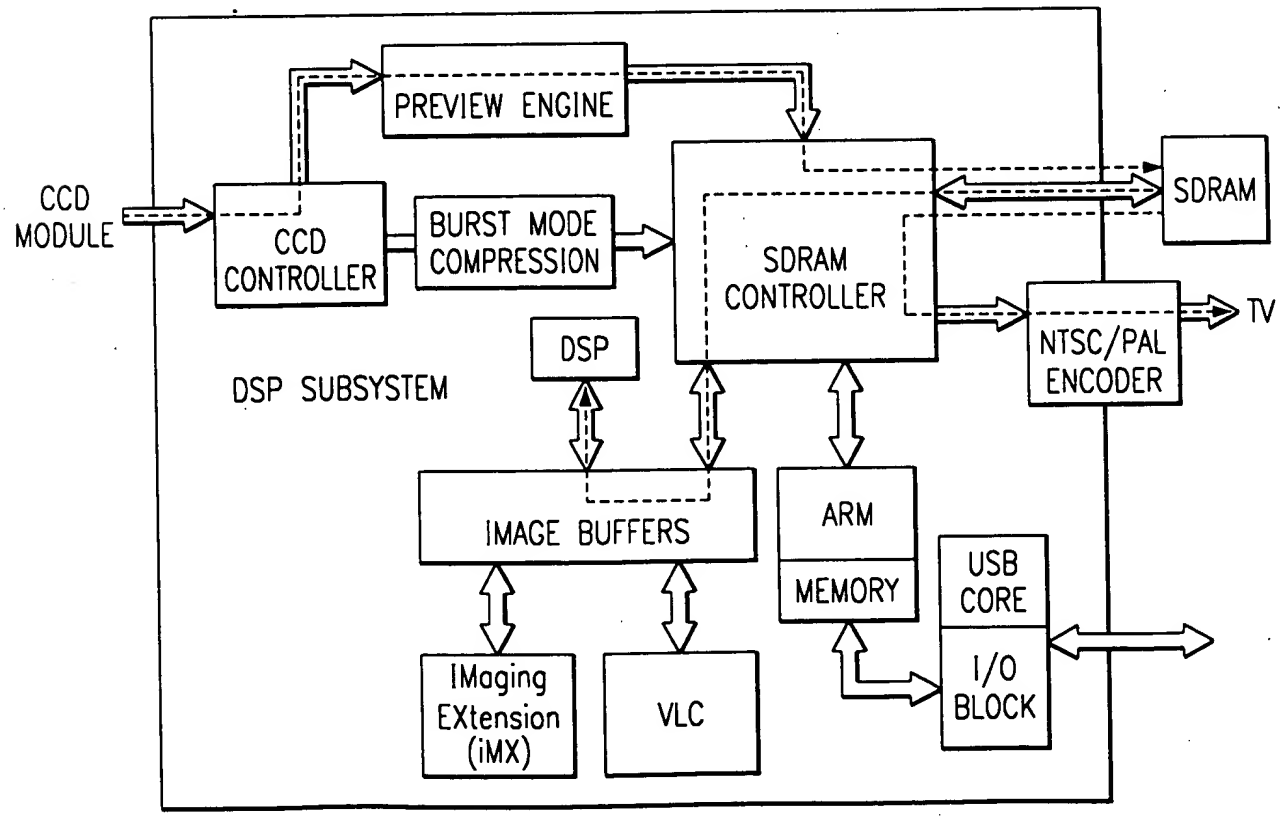

PREVIEW ENGINE
CCD MODULE
CCD CONTROLLER
BURST MODE COMPRESSION
SDRAM CONTROLLER
SDRAM
TV
NTSC/PAL ENCODER
DSP
DSP SUBSYSTEM
IMAGE BUFFERS
ARM
MEMORY
USB CORE
I/O BLOCK
IMaging EXtension (iMX)
VLC

FIG. 2

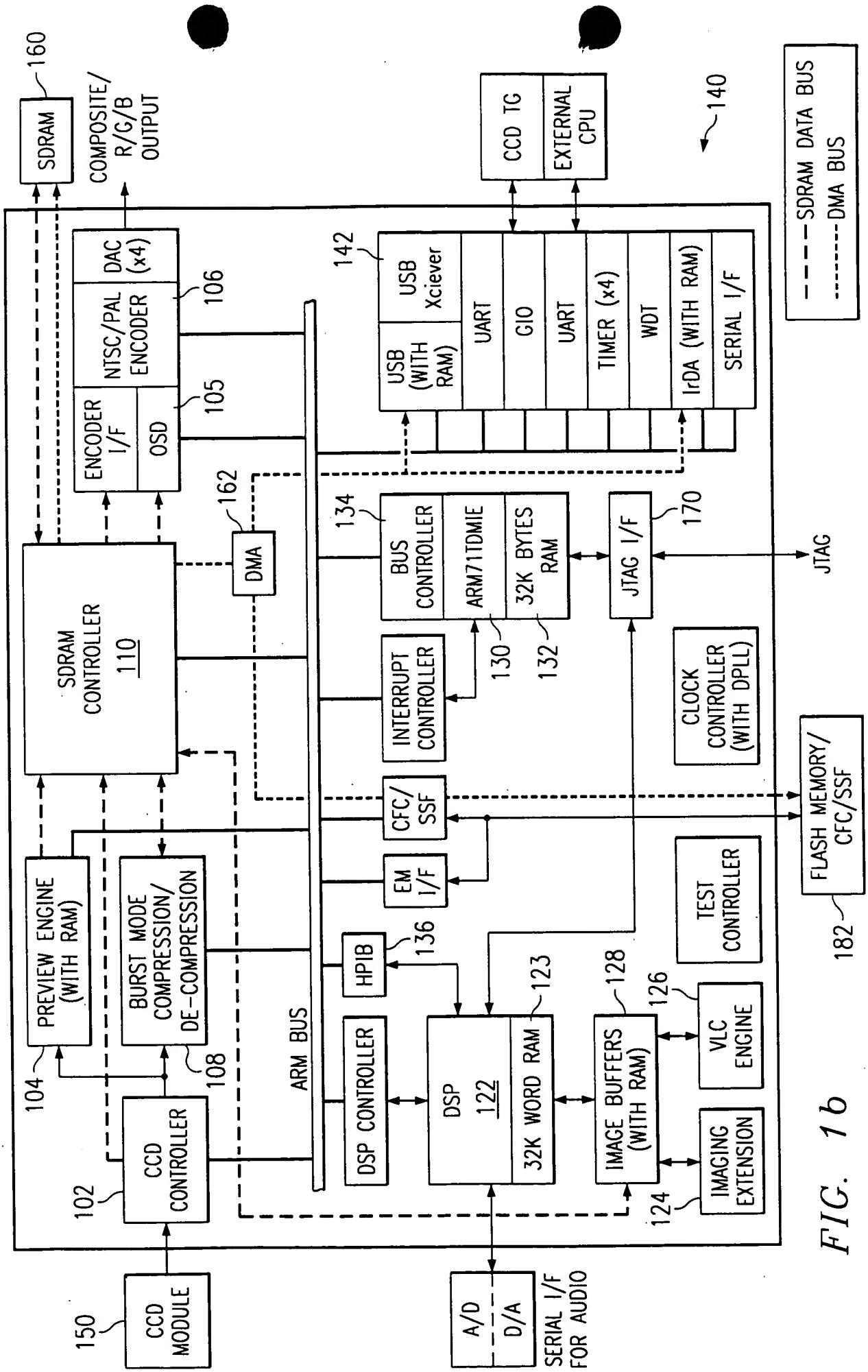

SDRAM
160
COMPOSITE/ R/G/B OUTPUT
DAC (x4)
NTSC/PAL ENCODER
106
ENCODER I/F
OSD
105
162
DMA
SDRAM CONTROLLER 110
104
PREVIEW ENGINE (WITH RAM)
BURST MODE COMPRESSION/ DE-COMPRESSION
108
CCD CONTROLLER
102
CCD MODULE
150
ARM BUS
HPIB
136
DSP CONTROLLER
DSP 122
32K WORD RAM
123
IMAGE BUFFERS (WITH RAM)
128
126
VLC ENGINE
IMAGING EXTENSION
124
A/D D/A
SERIAL I/F FOR AUDIO
CFC/ SSF
EM I/F
INTERRUPT CONTROLLER
BUS CONTROLLER
ARM7TDMIE
32K BYTES RAM
134
130
132
JTAG I/F
170
JTAG
CLOCK CONTROLLER (WITH DPLL)
TEST CONTROLLER
FLASH MEMORY/ CFC/SSF
182
CCD TG
EXTERNAL CPU
140
142
USB (WITH RAM)
USB Xciever
UART
GIO
UART
TIMER (x4)
WDT
IrDA (WITH RAM)
SERIAL I/F
SDRAM DATA BUS
DMA BUS

FIG. 1b

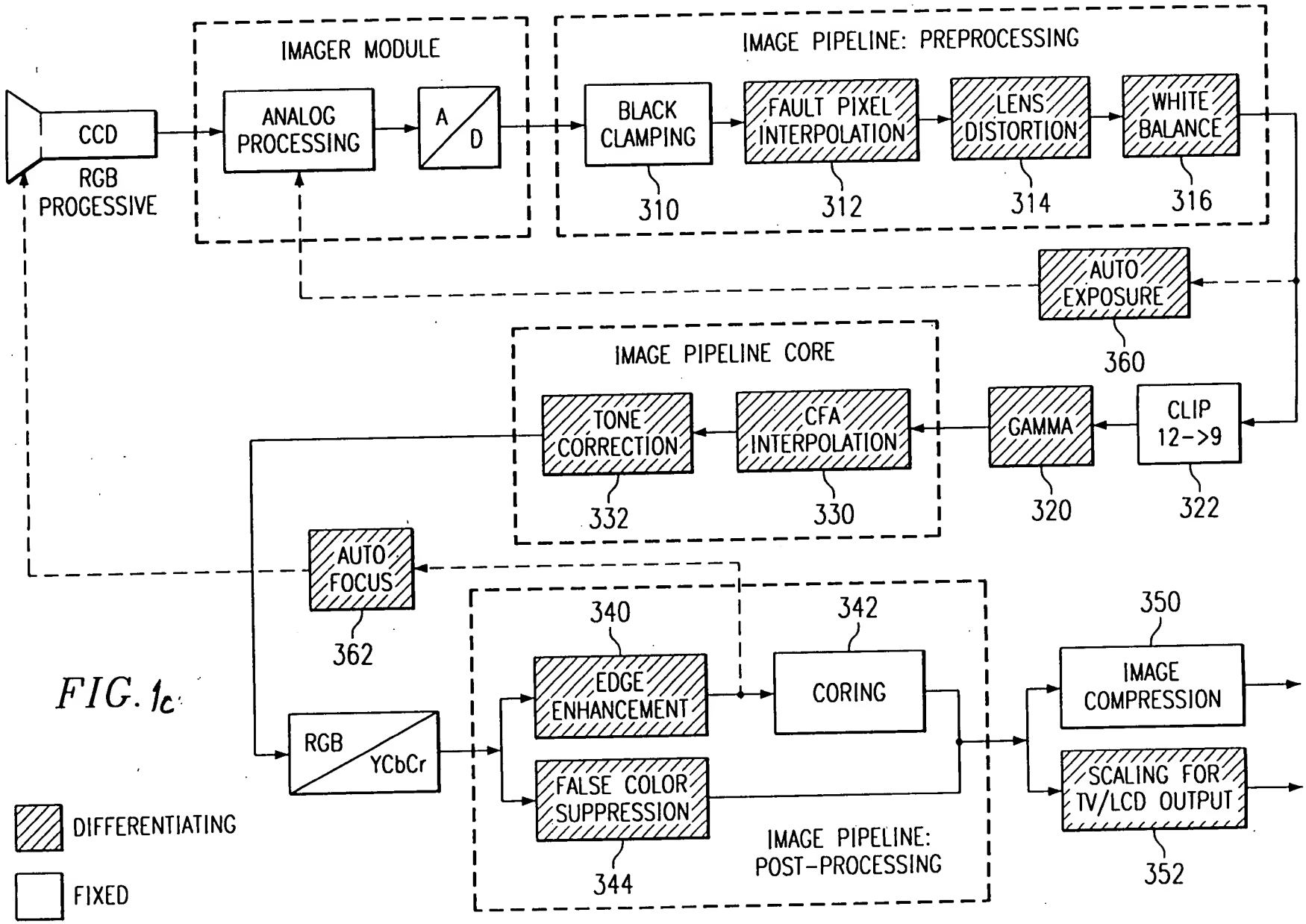


FIG. 1c

TI-28764

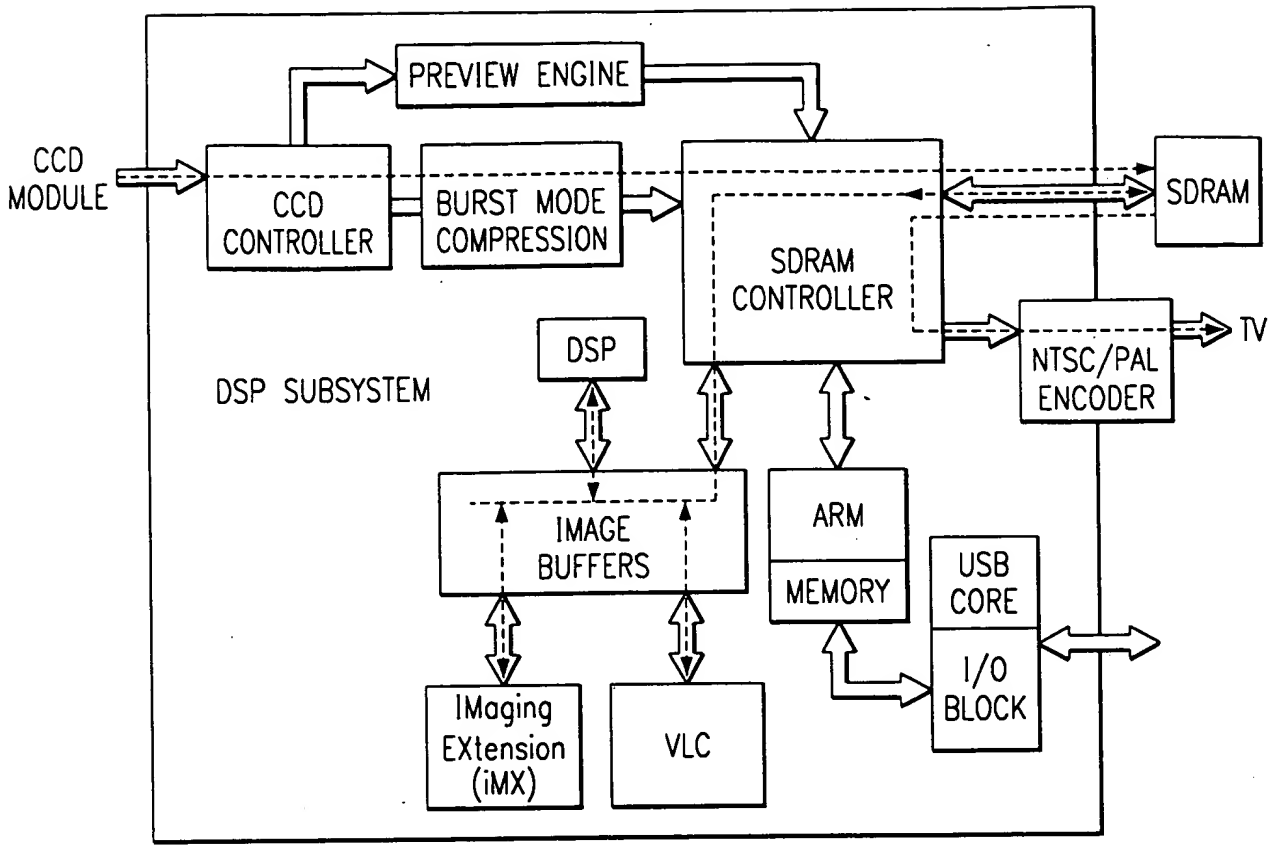

PREVIEW ENGINE
CCD MODULE
CCD CONTROLLER
BURST MODE COMPRESSION
SDRAM CONTROLLER
SDRAM
TV
NTSC/PAL ENCODER
DSP
DSP SUBSYSTEM
IMAGE BUFFERS
ARM
MEMORY
USB CORE
I/O BLOCK
IMaging EXtension (iMX)
VLC

FIG. 3a

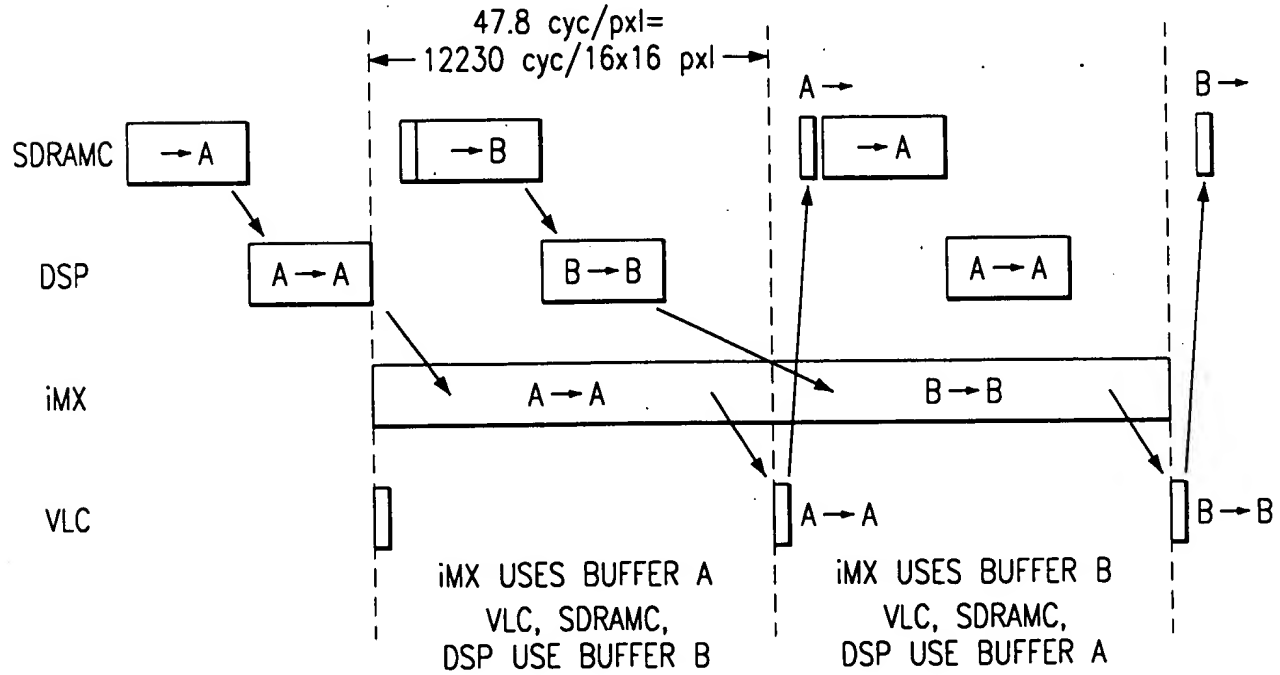

47.8 cyc/pxl=
12230 cyc/16x16 pxl
SDRAMC
DSP
iMX
VLC
A→A
B→B
iMX USES BUFFER A
VLC, SDRAMC,
DSP USE BUFFER B
iMX USES BUFFER B
VLC, SDRAMC,
DSP USE BUFFER A

FIG. 3b

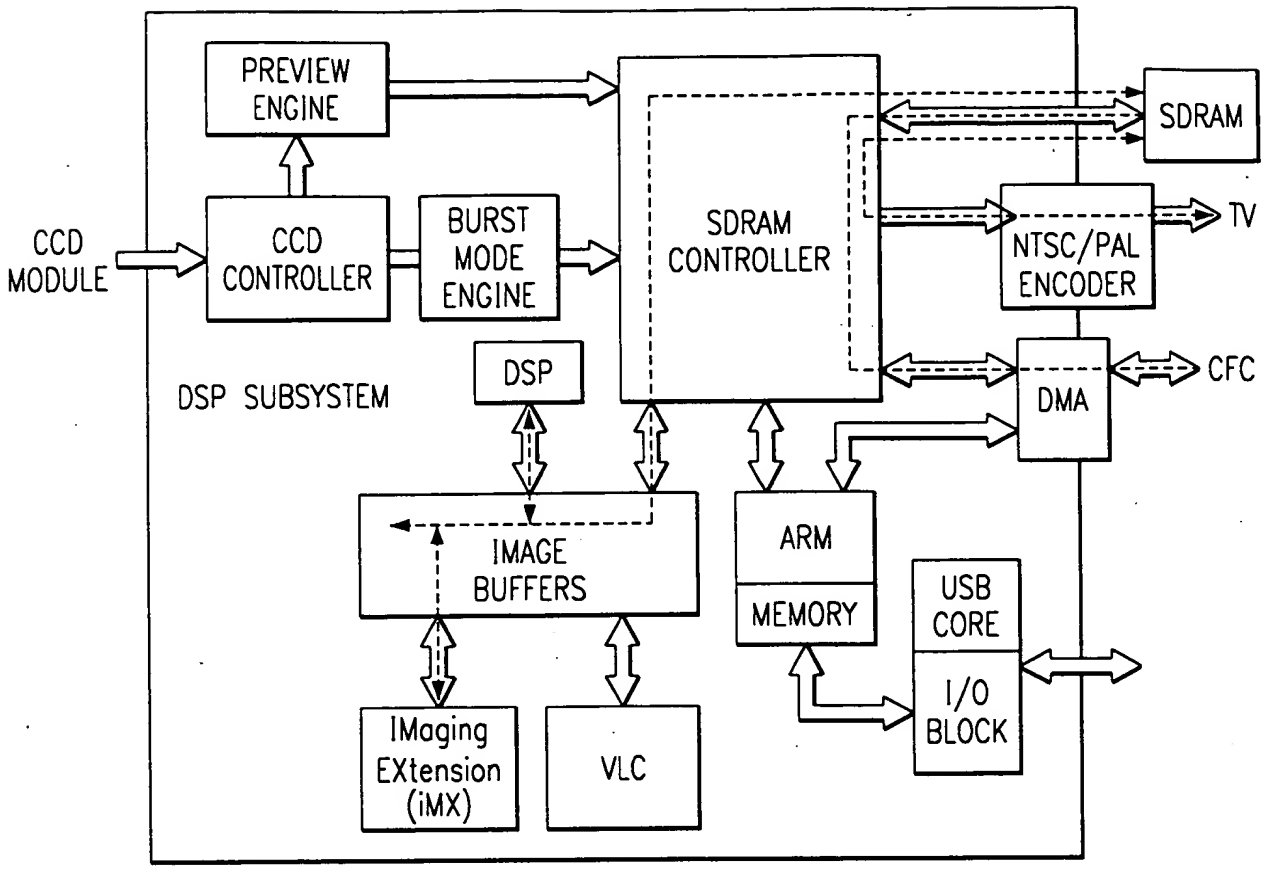

PREVIEW ENGINE
SDRAM
CCD MODULE
CCD CONTROLLER
BURST MODE ENGINE
SDRAM CONTROLLER
NTSC/PAL ENCODER
TV
DSP SUBSYSTEM
DSP
DMA
CFC
IMAGE BUFFERS
ARM
MEMORY
USB CORE
I/O BLOCK
IMaging EXtension (iMX)
VLC

FIG. 4

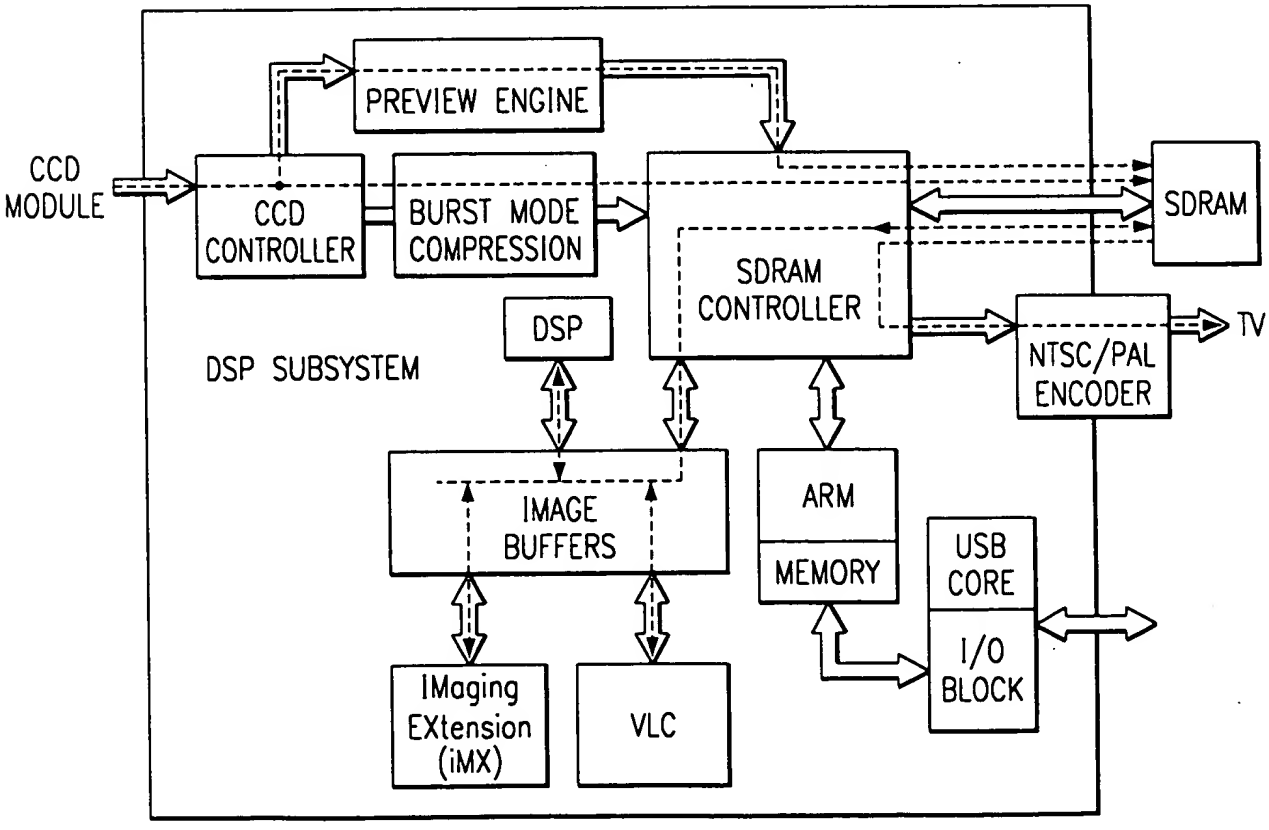

PREVIEW ENGINE
CCD MODULE
CCD CONTROLLER
BURST MODE COMPRESSION
SDRAM
SDRAM CONTROLLER
DSP
TV
NTSC/PAL ENCODER
DSP SUBSYSTEM
IMAGE BUFFERS
ARM
MEMORY
USB CORE
I/O BLOCK
IMaging EXtension (iMX)
VLC

FIG. 5

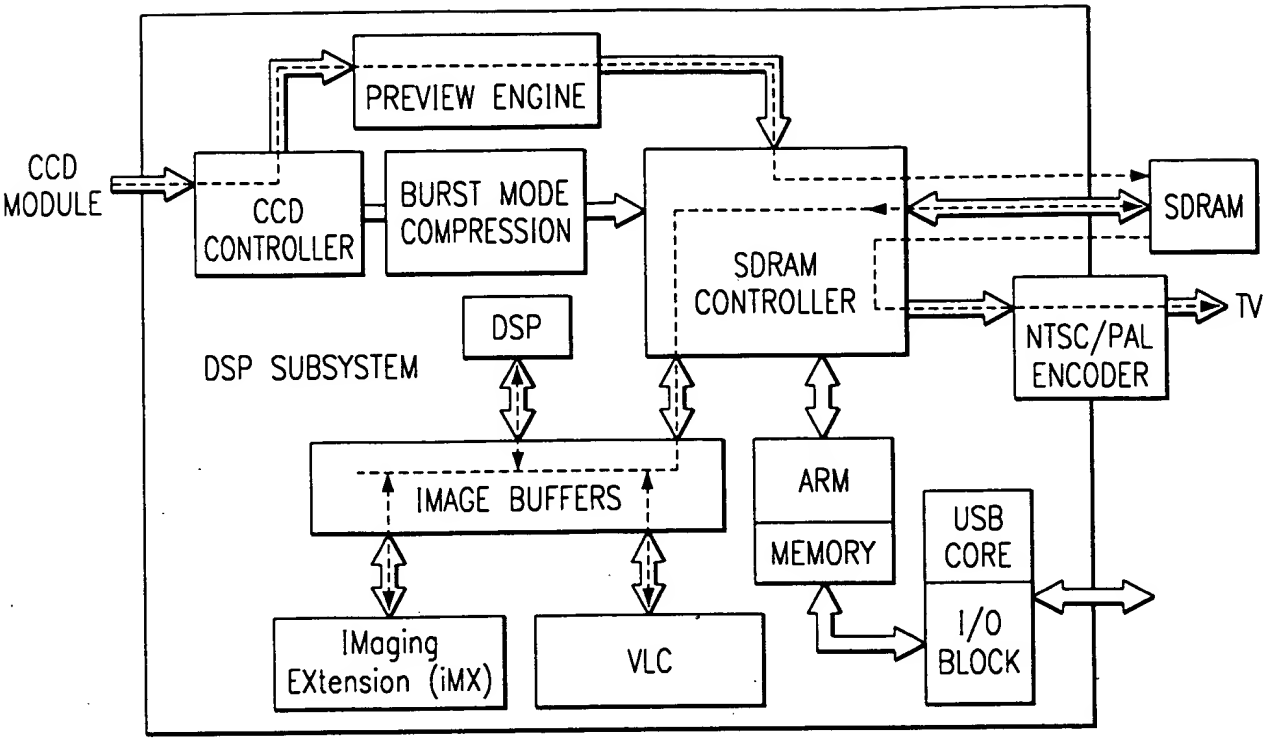


FIG. 6

R	G	R	G
G	B	G	B
R	G	R	G
G	B	G	B

FIG. 7a

Ye	Cy	Ye	Cy
G	Mg	G	Mg
Ye	Cy	Ye	Cy
G	Mg	G	Mg

FIG. 7b

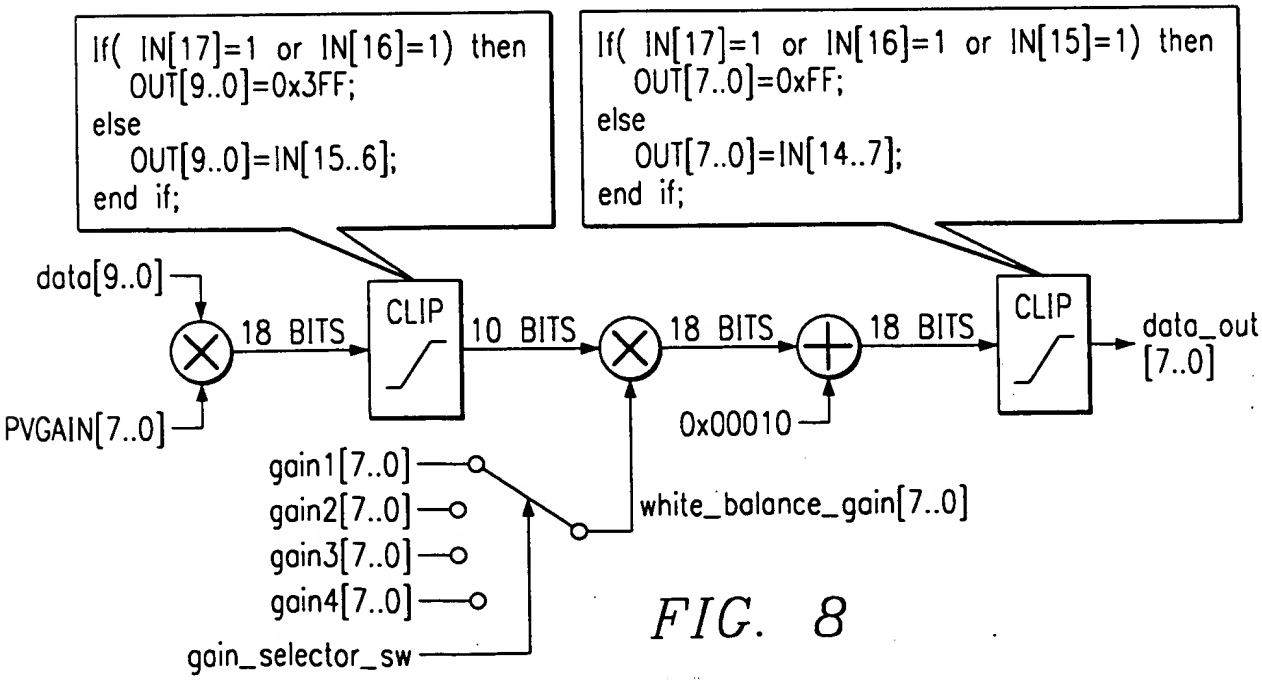


FIG. 8

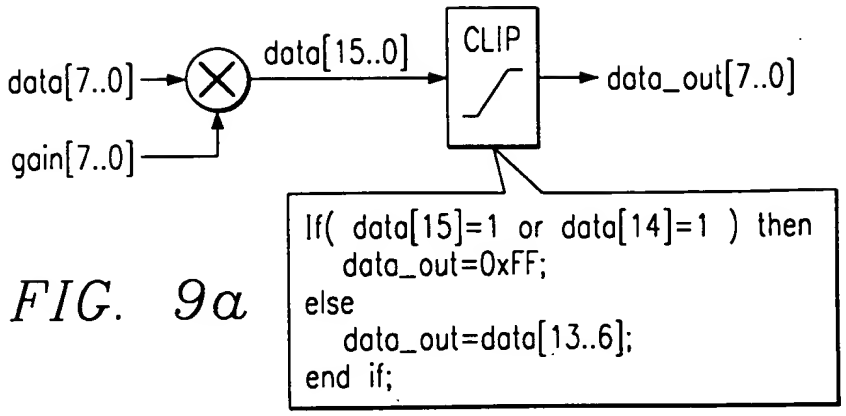


FIG. 9a

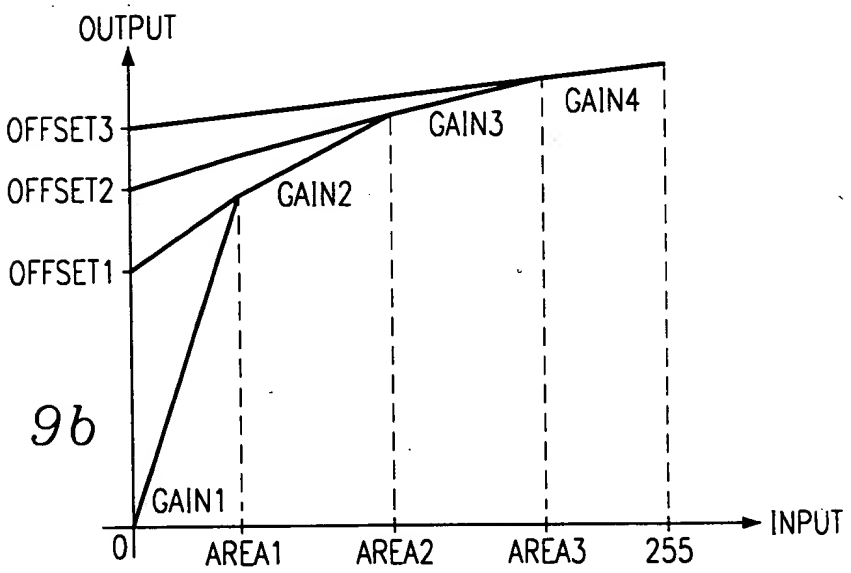


FIG. 9b

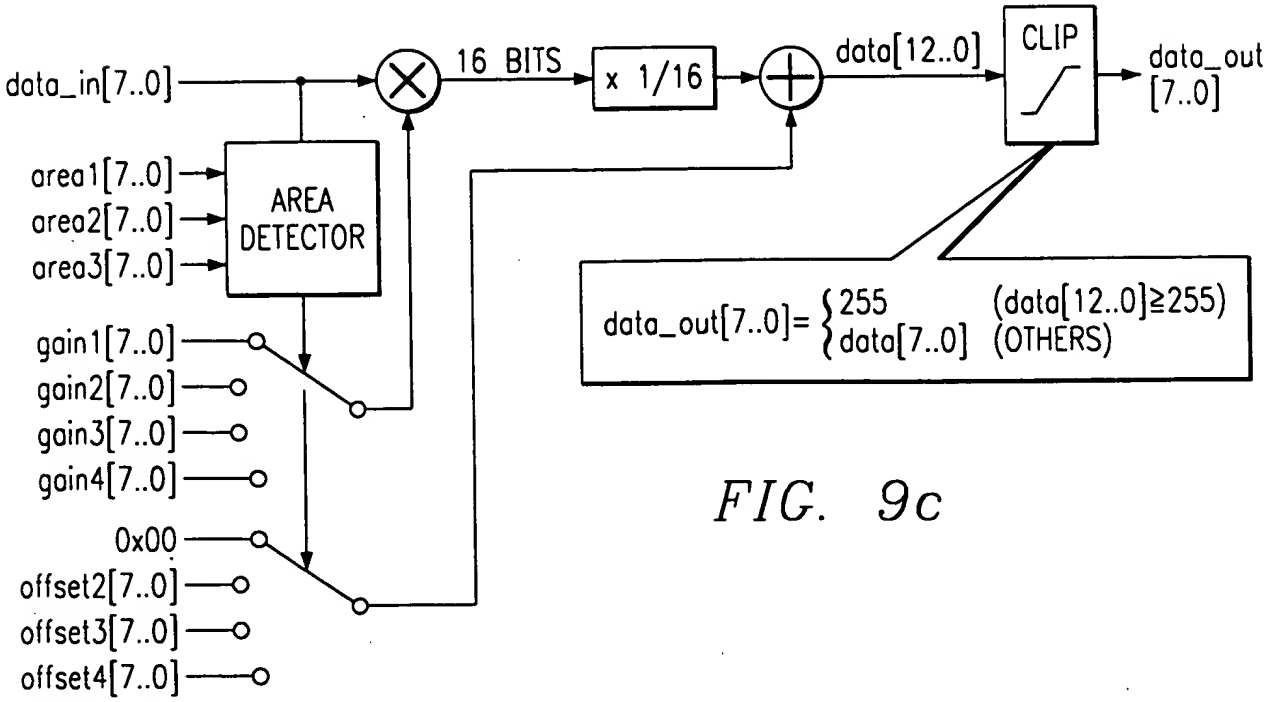


FIG. 9c

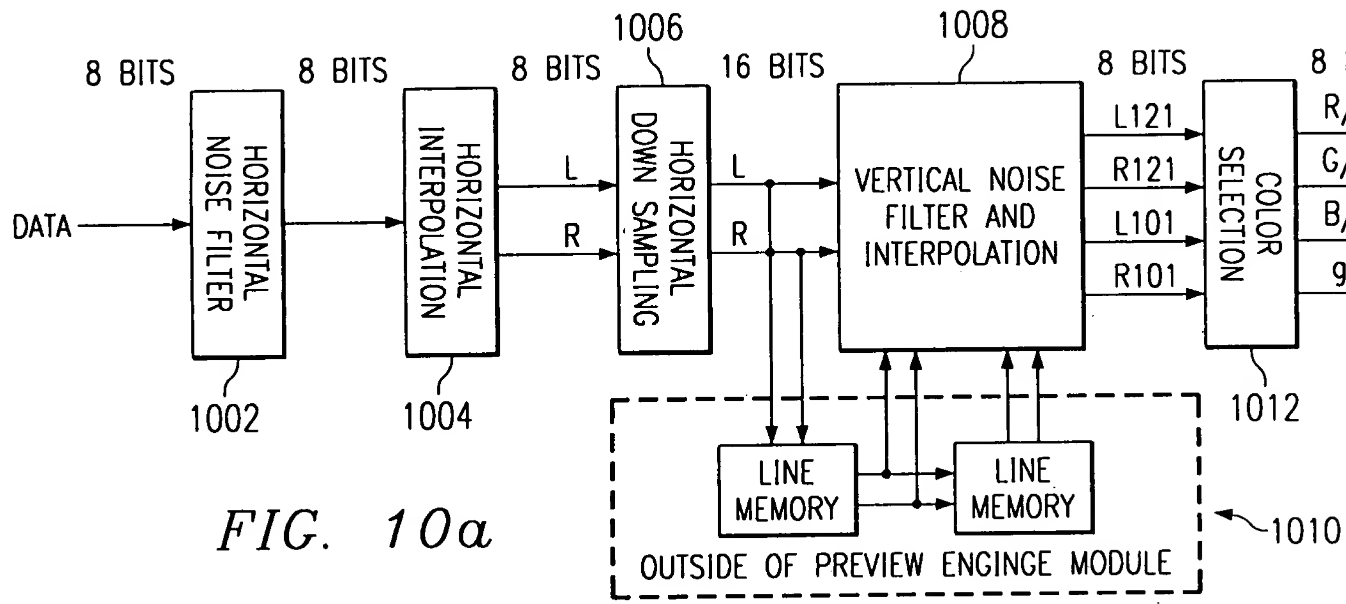


FIG. 10a

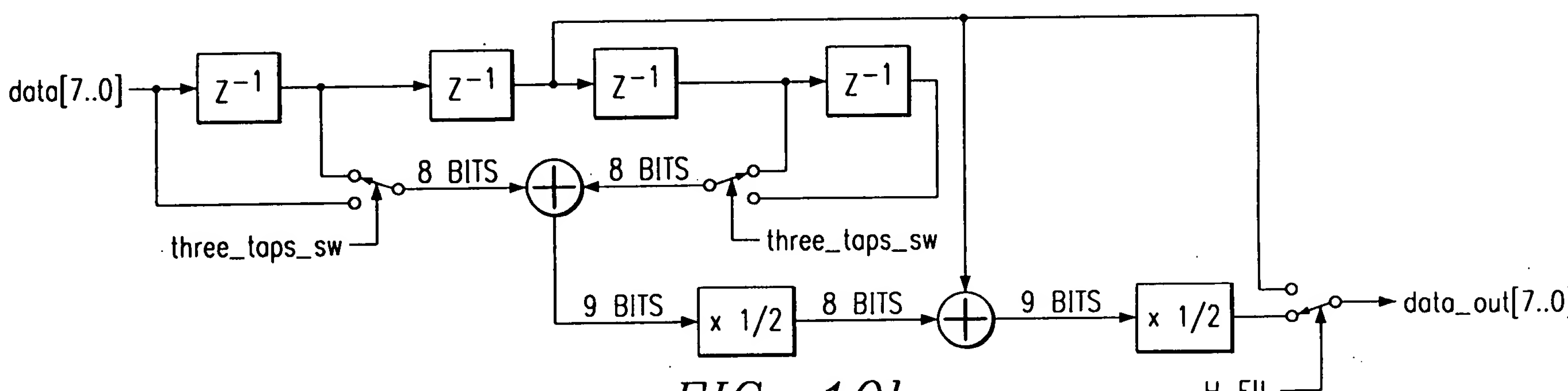


FIG. 10b

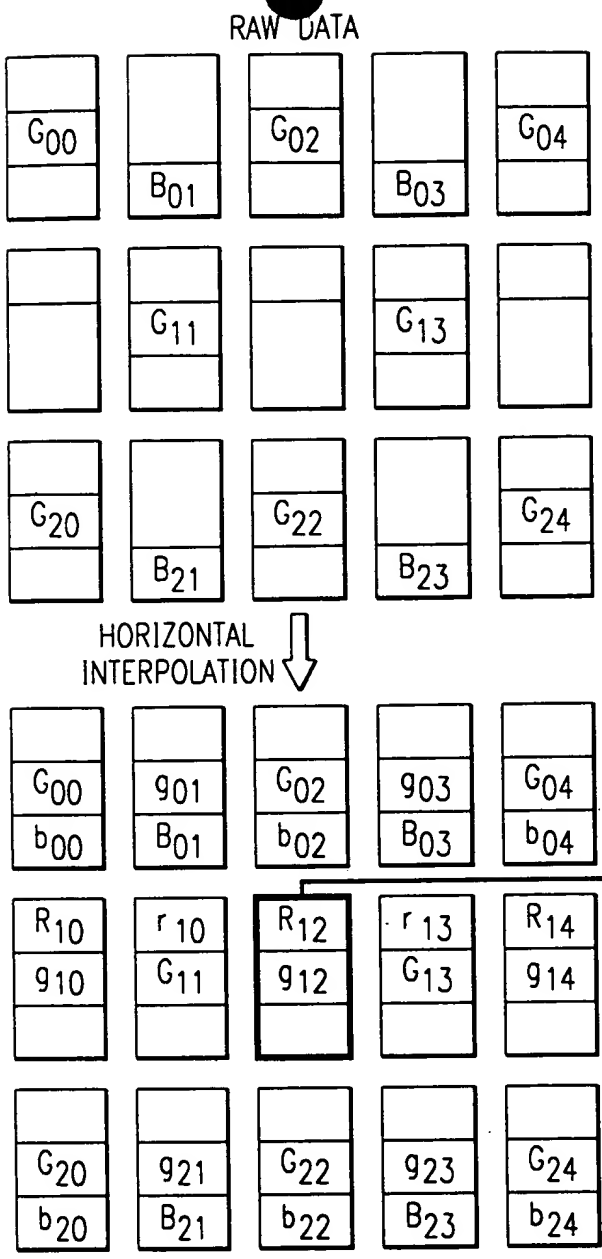


FIG. 10c

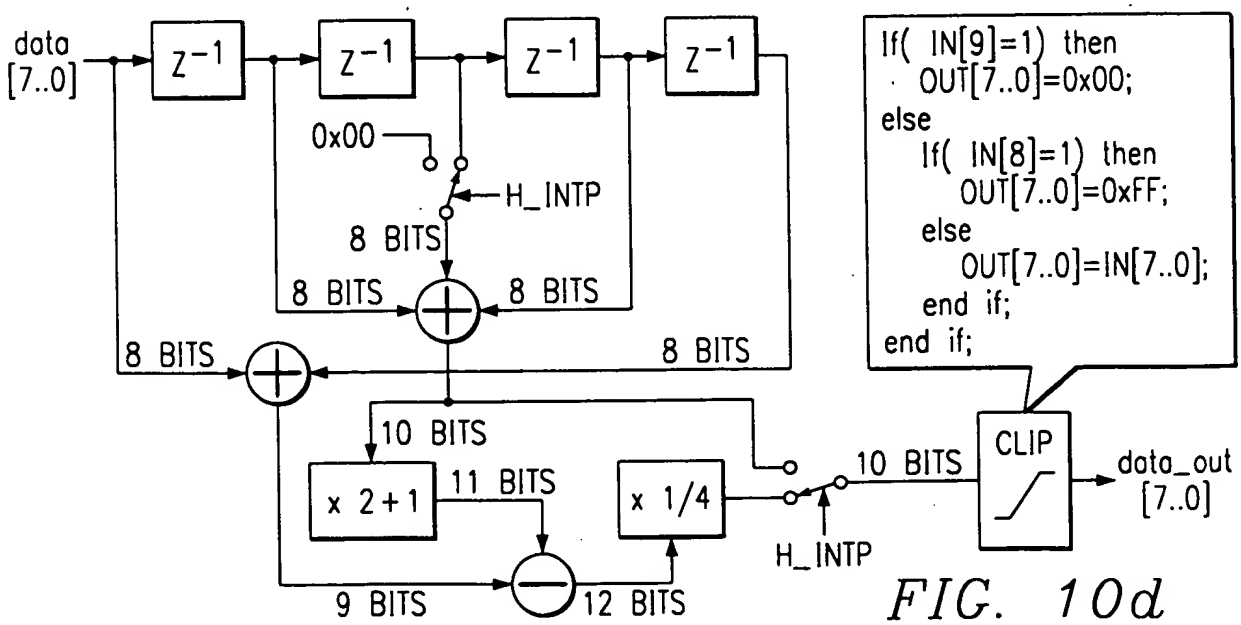


FIG. 10d

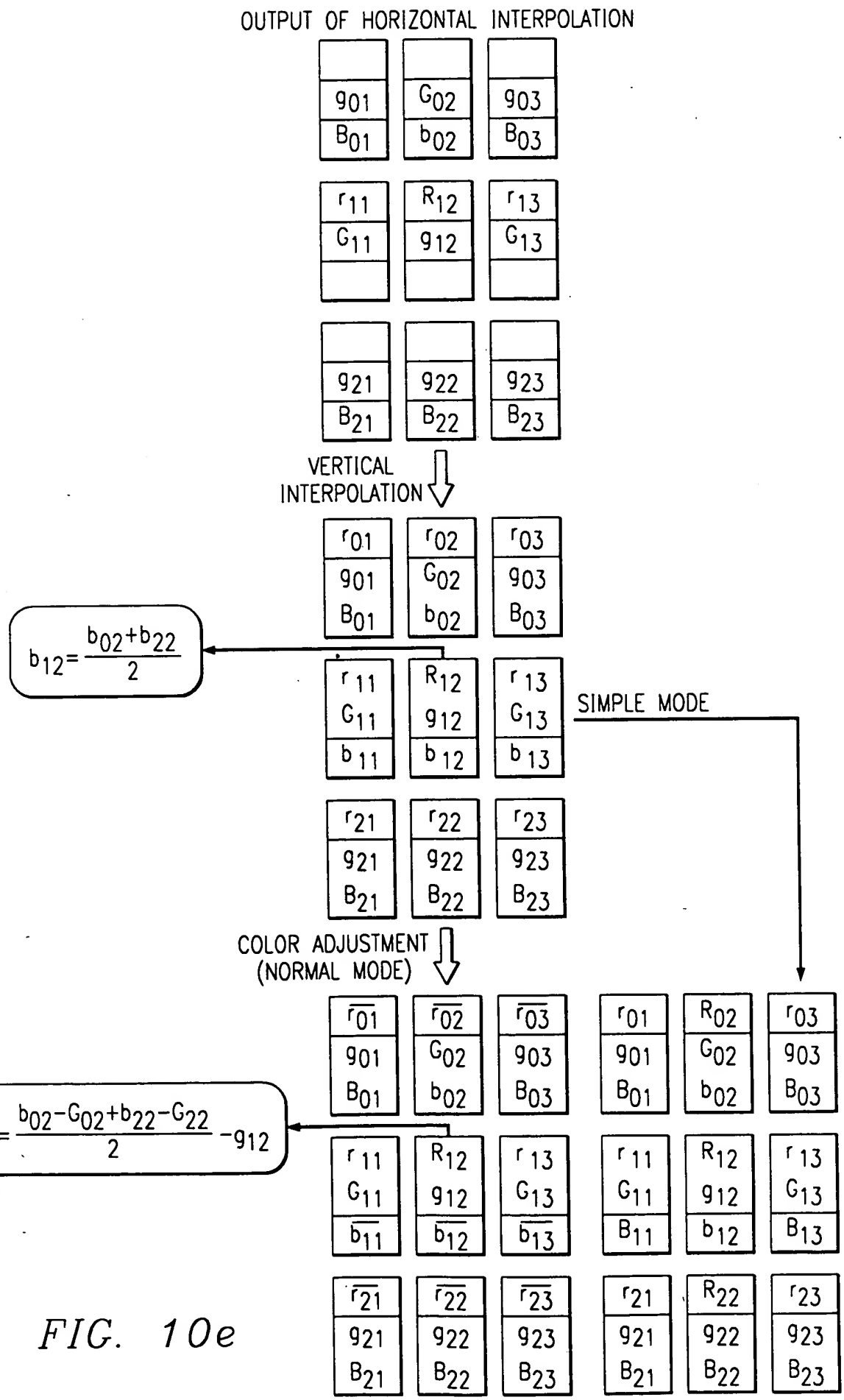

OUTPUT OF HORIZONTAL INTERPOLATION
VERTICAL INTERPOLATION
$b_{12}=\frac{b_{02}+b_{22}}{2}$
SIMPLE MODE
COLOR ADJUSTMENT (NORMAL MODE)
$\overline{b_{12}}=\frac{b_{02}-G_{02}+b_{22}-G_{22}}{2}-g_{12}$

FIG. 10e

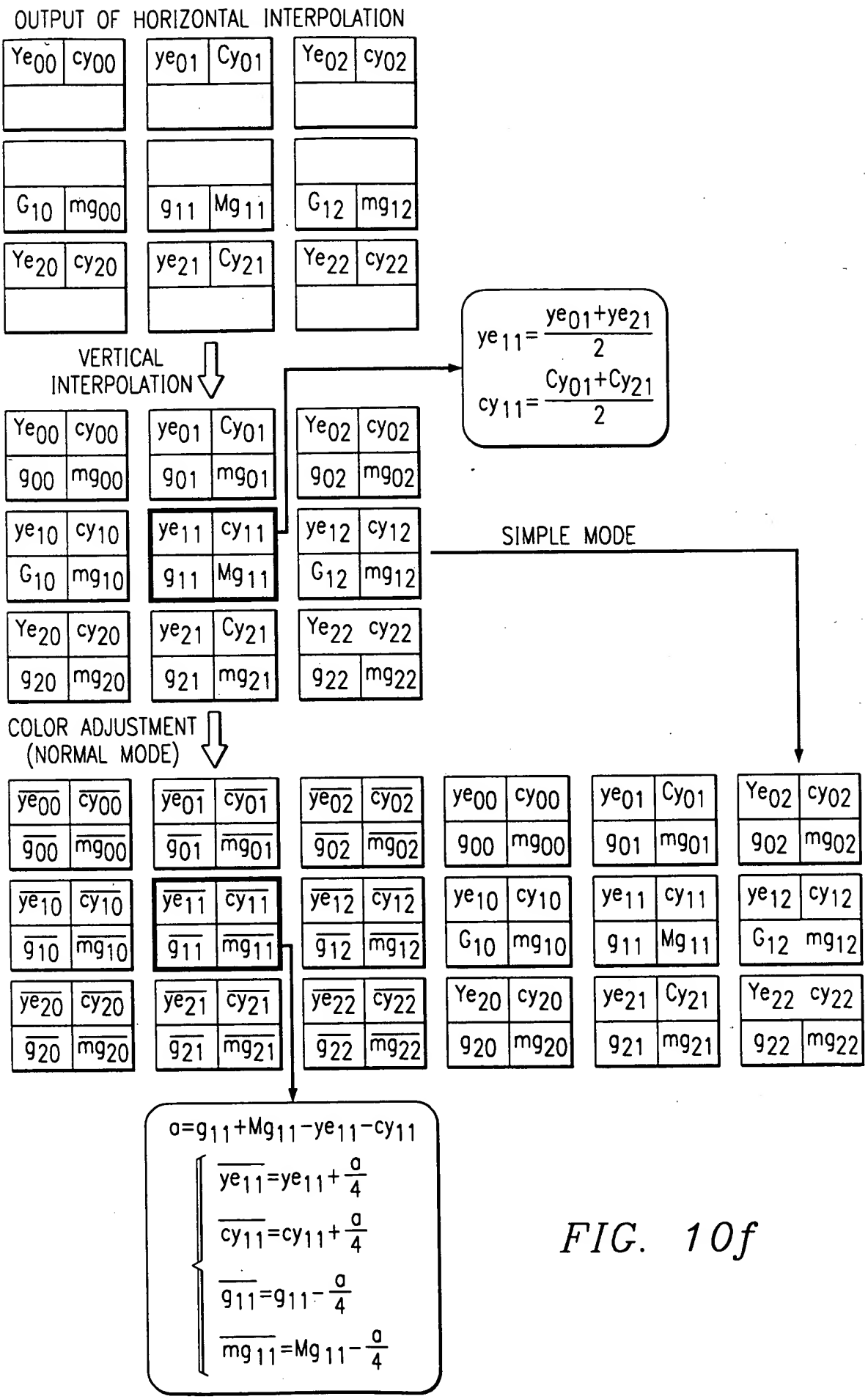
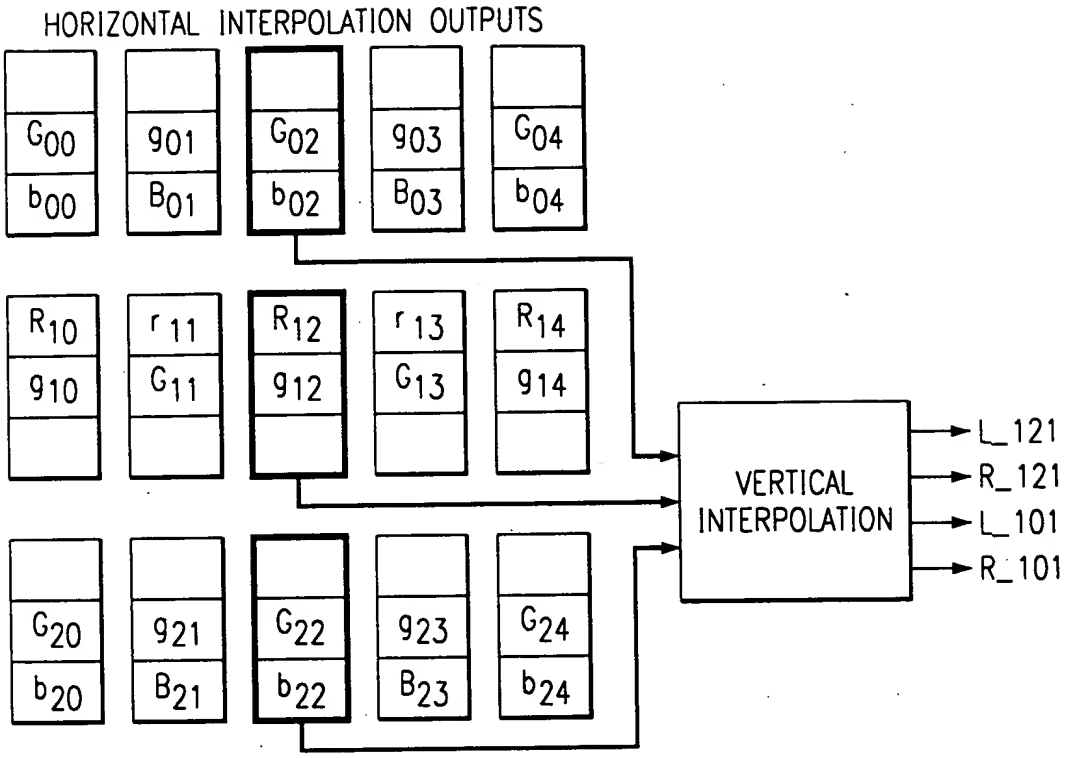

OUTPUT OF HORIZONTAL INTERPOLATION
VERTICAL INTERPOLATION
$ye_{11}=\frac{ye_{01}+ye_{21}}{2}$
$cy_{11}=\frac{Cy_{01}+Cy_{21}}{2}$
SIMPLE MODE
COLOR ADJUSTMENT (NORMAL MODE)
$a=g_{11}+Mg_{11}-ye_{11}-cy_{11}$
$\overline{ye_{11}}=ye_{11}+\frac{a}{4}$
$\overline{cy_{11}}=cy_{11}+\frac{a}{4}$
$\overline{g_{11}}=g_{11}-\frac{a}{4}$
$\overline{mg_{11}}=Mg_{11}-\frac{a}{4}$

FIG. 10f



NOISE FILTER = OFF

$$\begin{cases} L\_121 = R_{12} \\ R\_121 = g_{12} \\ L\_101 = \dfrac{G_{02}+G_{22}}{2} \\ R\_101 = \dfrac{b_{02}+b_{22}}{2} \end{cases}$$

NOISE FILTER = ON

$$\begin{cases} L\_121 = R_{12} - g_{12} + \dfrac{G_{02}+2g_{12}+G_{22}}{4} \\ R\_121 = \dfrac{G_{02}+2g_{12}+G_{22}}{4} \\ L\_101 = \dfrac{G_{02}+G_{22}}{2} \\ R\_101 = \dfrac{b_{02}+b_{22}}{2} \end{cases}$$

FIG. 10g

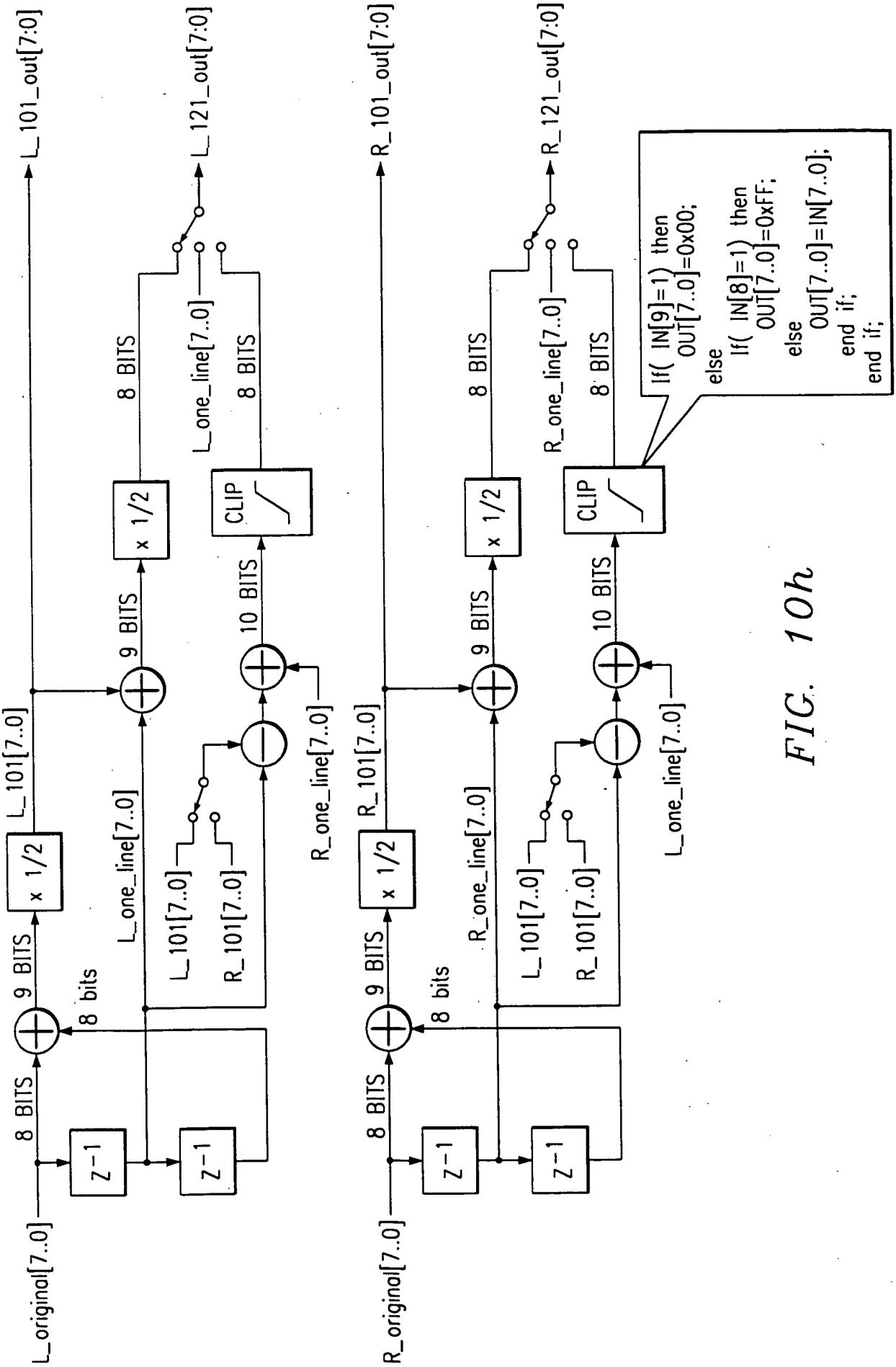
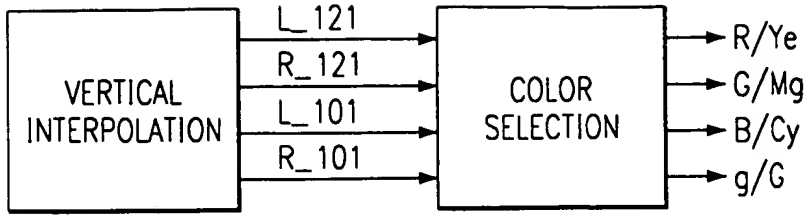

L_original[7..0]
R_original[7..0]
8 BITS
9 BITS
10 BITS
8 bits
Z-1
x 1/2
CLIP
L_101[7..0]
R_101[7..0]
L_one_line[7..0]
R_one_line[7..0]
L_101_out[7:0]
R_101_out[7:0]
L_121_out[7:0]
R_121_out[7:0]
If(IN[9]=1) then
OUT[7..0]=0x00;
else
If(IN[8]=1) then
OUT[7..0]=0xFF;
else
OUT[7..0]=IN[7..0];
end if;
end if;

FIG. 10h



NOISE FILTER = OFF

$$\begin{cases} R/Ye = R_{12} \\ G/Mg = g_{12} \\ g/Cy = \dfrac{G_{02}+G_{22}}{2} \\ B/Cy = \dfrac{b_{02}+b_{22}}{2} \end{cases}$$

NOISE FILTER = ON

$$\begin{cases} R/Ye = R_{12} - g_{12} + \dfrac{G_{02}+2g_{12}+G_{22}}{4} \\ G/Mg = \dfrac{G_{02}+2g_{12}+G_{22}}{4} \\ g/Cy = \dfrac{G_{02}+G_{22}}{2} \\ B/Cy = \dfrac{b_{02}+b_{22}}{2} \end{cases}$$

FIG. 10i

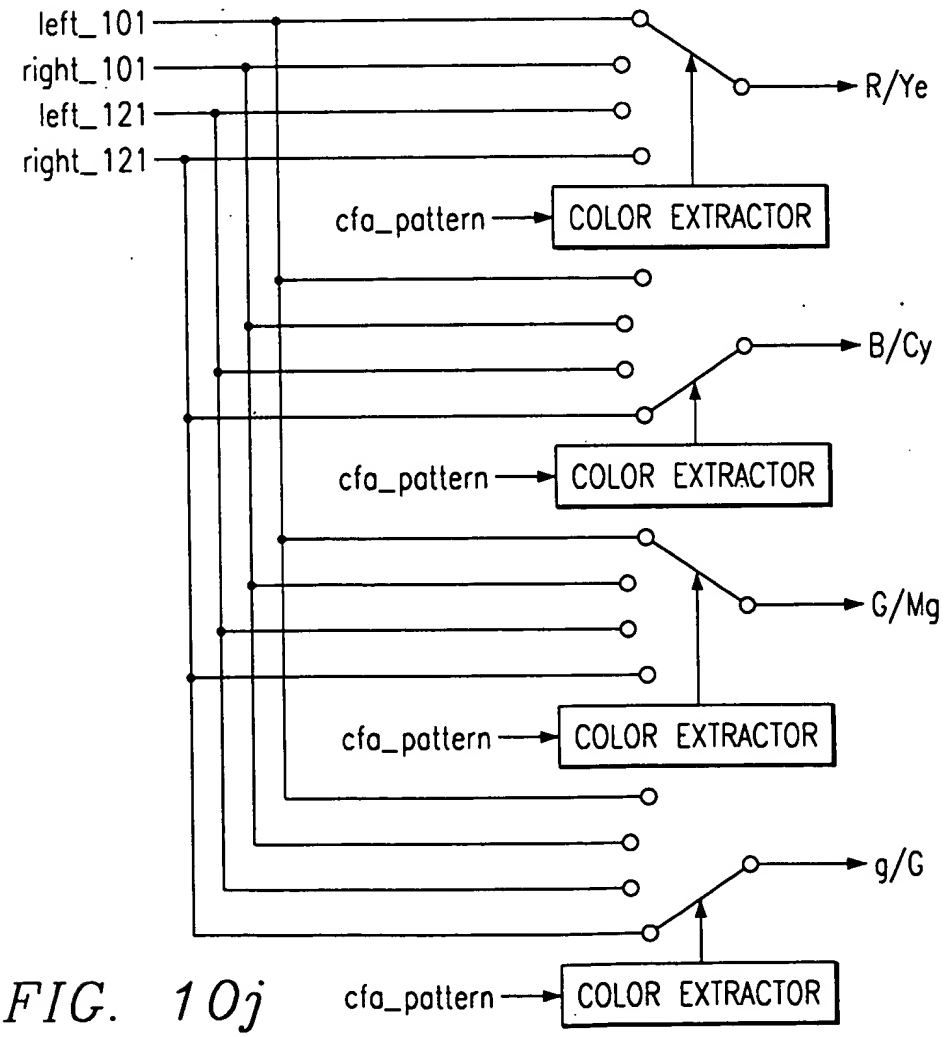


FIG. 10j

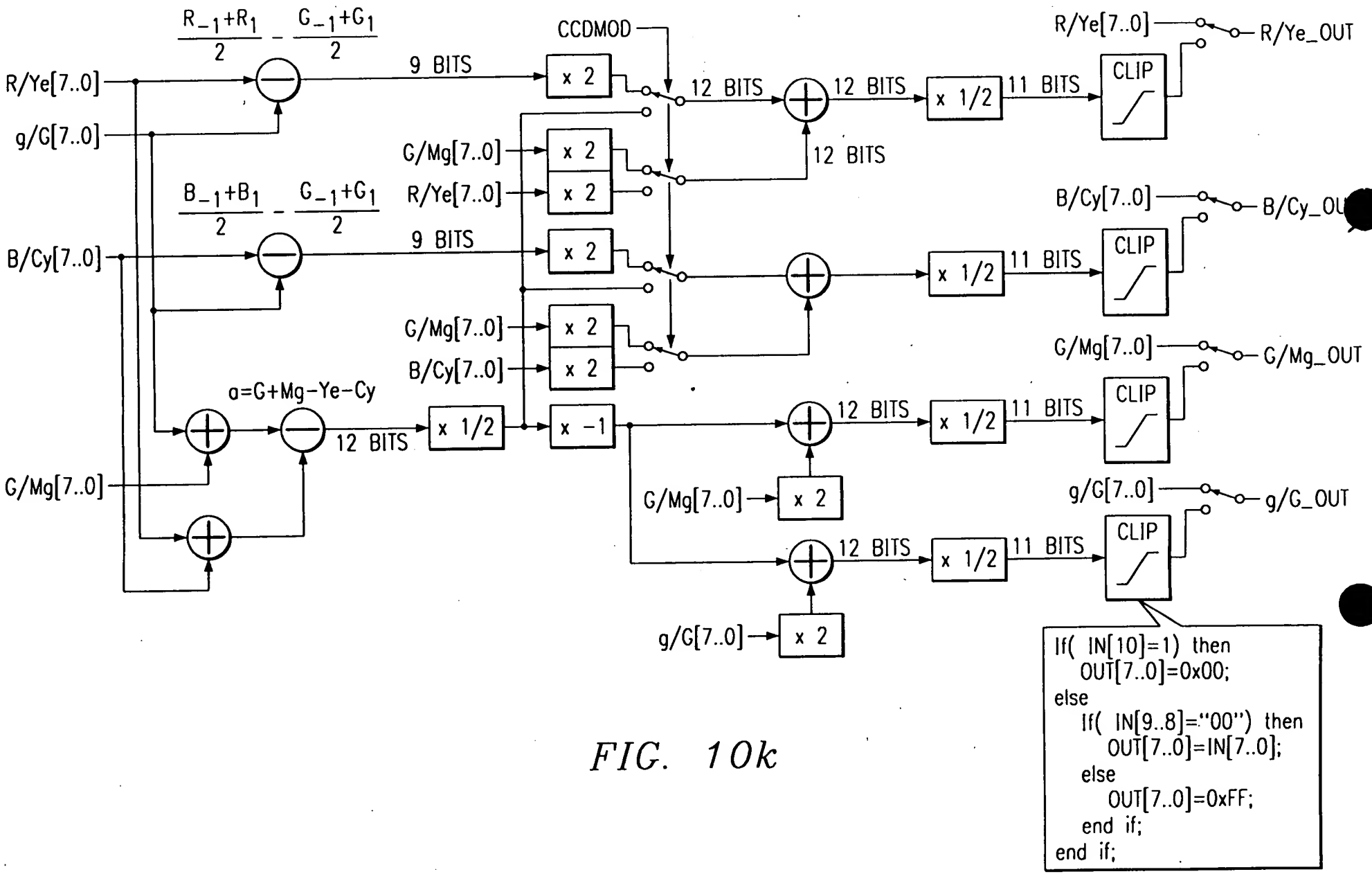

R/Ye[7..0]
g/G[7..0]
B/Cy[7..0]
G/Mg[7..0]
(R_-1+R_1)/2 - (G_-1+G_1)/2
(B_-1+B_1)/2 - (G_-1+G_1)/2
a=G+Mg-Ye-Cy
9 BITS
12 BITS
CCDMOD
x 2
x 1/2
x -1
11 BITS
CLIP
R/Ye_OUT
B/Cy_OUT
G/Mg_OUT
g/G_OUT
If(IN[10]=1) then
OUT[7..0]=0x00;
else
If(IN[9..8]="00") then
OUT[7..0]=IN[7..0];
else
OUT[7..0]=0xFF;
end if;
end if;

FIG. 10k

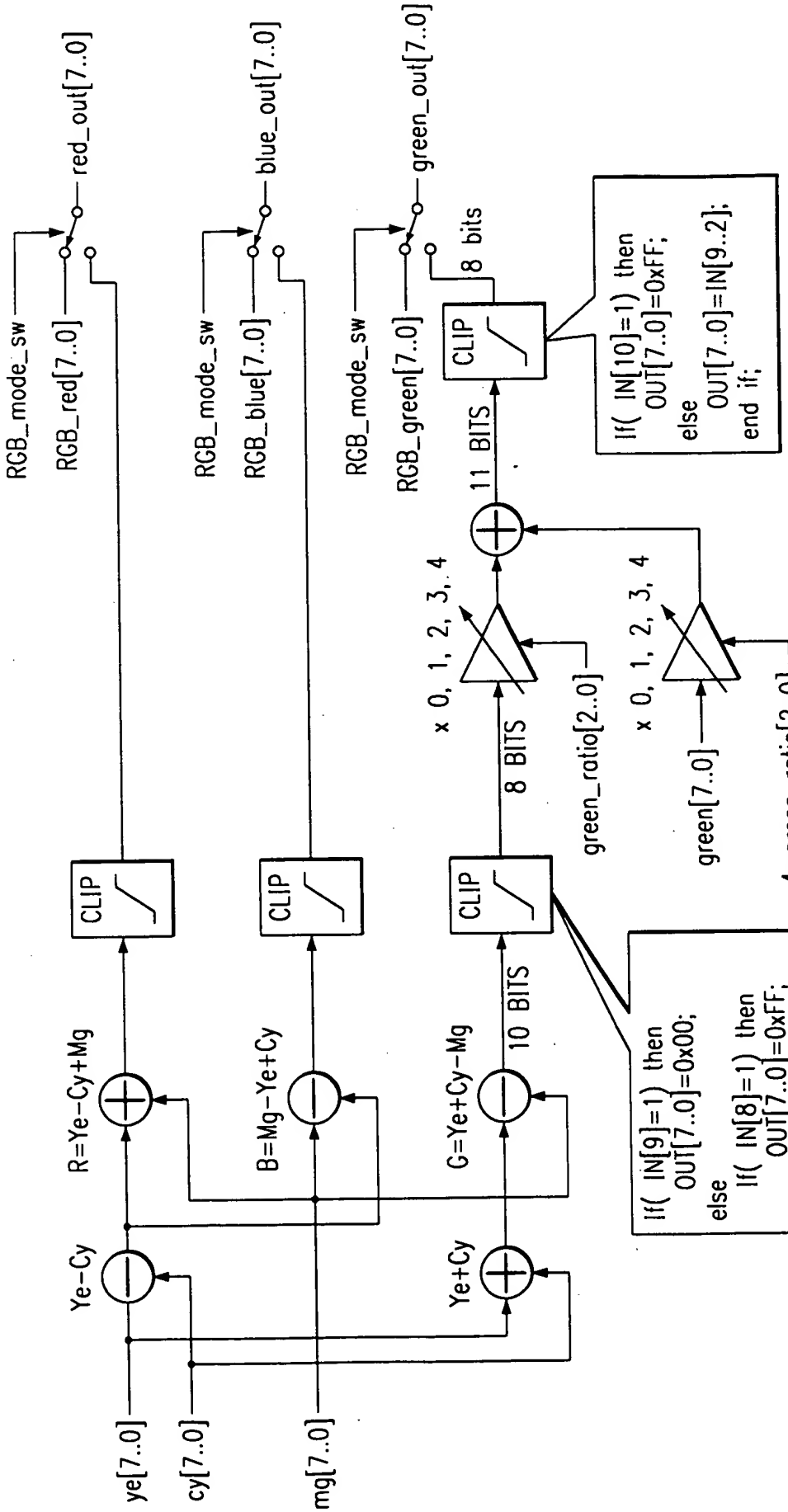

ye[7..0]
cy[7..0]
mg[7..0]
Ye−Cy
Ye+Cy
R=Ye−Cy+Mg
B=Mg−Ye+Cy
G=Ye+Cy−Mg
CLIP
CLIP
CLIP
10 BITS
8 BITS
11 BITS
8 bits
x 0, 1, 2, 3, 4
x 0, 1, 2, 3, 4
green_ratio[2..0]
green[7..0]
4−green_ratio[2..0]
If(IN[9]=1) then
OUT[7..0]=0x00;
else
If(IN[8]=1) then
OUT[7..0]=0xFF;
else
OUT[7..0]=IN[7..0];
end if;
If(IN[10]=1) then
OUT[7..0]=0xFF;
else
OUT[7..0]=IN[9..2];
end if;
RGB_mode_sw
RGB_red[7..0]
red_out[7..0]
RGB_mode_sw
RGB_blue[7..0]
blue_out[7..0]
RGB_mode_sw
RGB_green[7..0]
green_out[7..0]

FIG. 10l

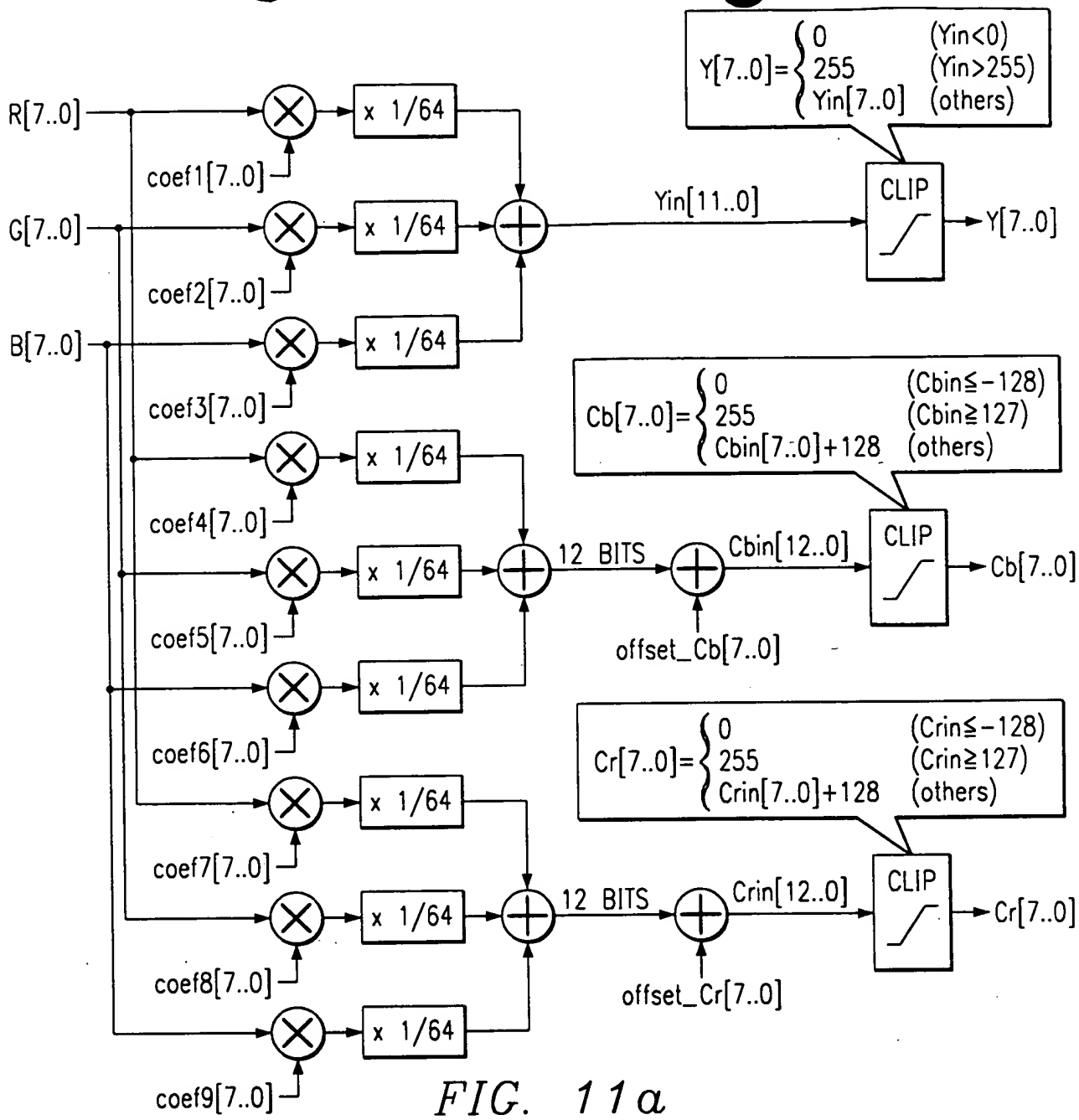


FIG. 11a

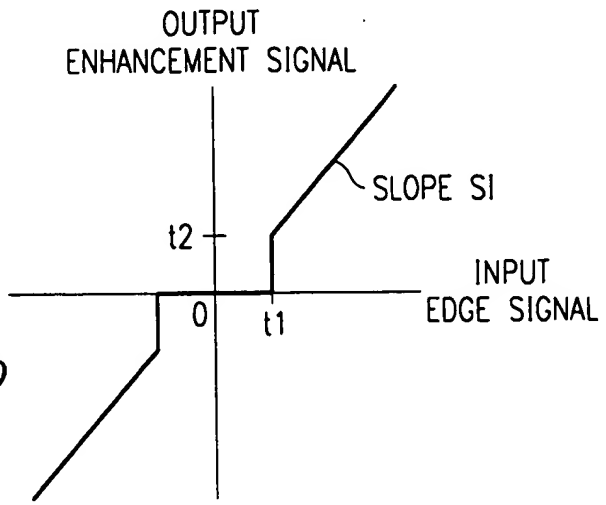
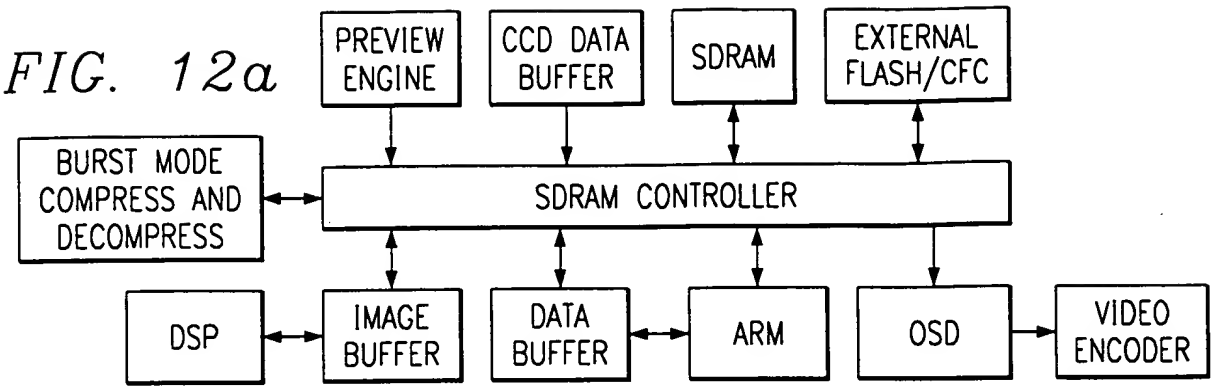


FIG. 11b

FIG. 12a



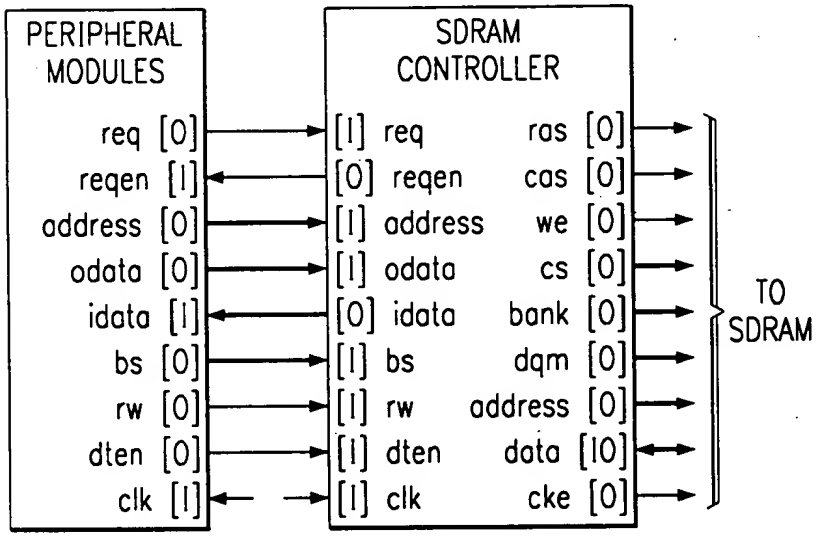


FIG. 12b

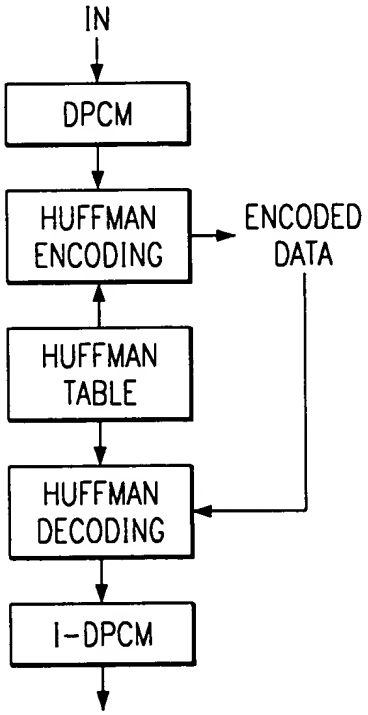


FIG. 13b

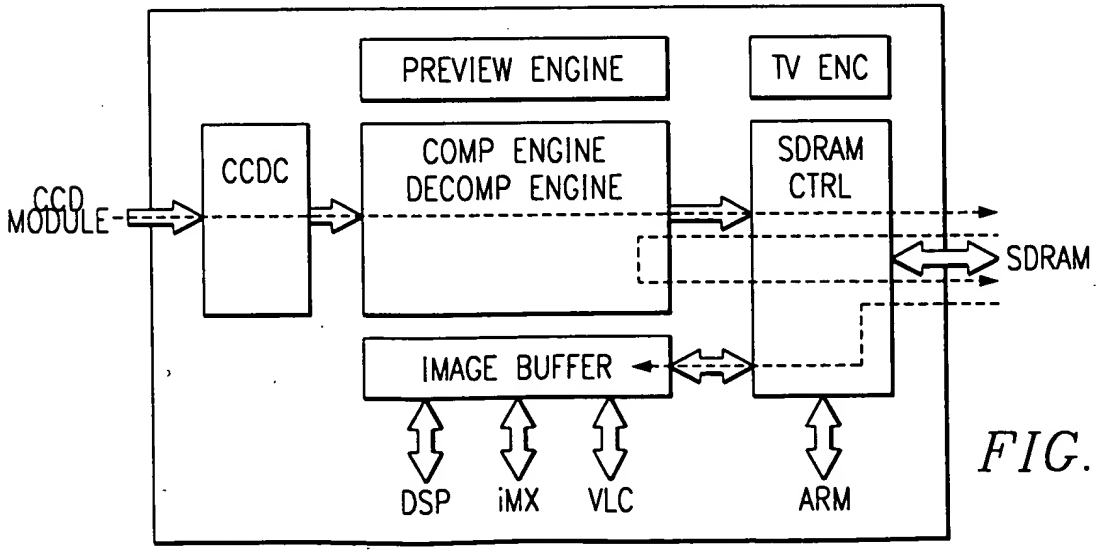


FIG. 13a

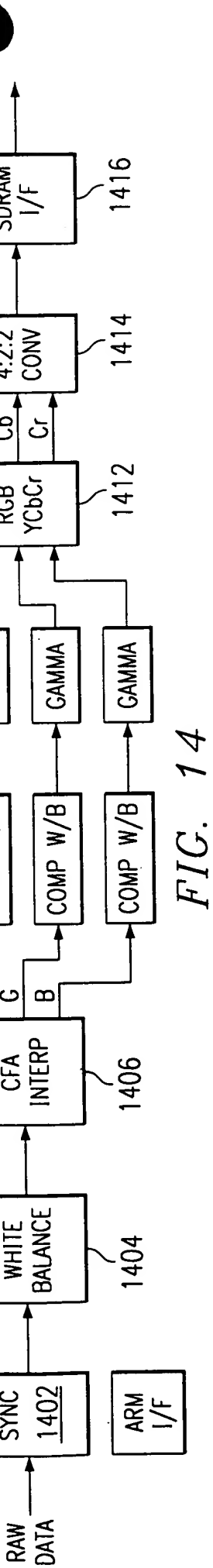

RAW DATA
10 BITS
SYNC 1402
10 BITS
WHITE BALANCE
1404
8 BITS
CFA INTERP
1406
R
G
B
8 BITS
1408
COMP W/B
COMP W/B
COMP W/B
8 BITS
1410
GAMMA
GAMMA
GAMMA
8 BITS
RGB YCbCr
1412
Y
Cb
Cr
8 BITS
4:2:2 CONV
1414
32 BITS
SDRAM I/F
1416
32 BITS
ARM I/F

FIG. 14

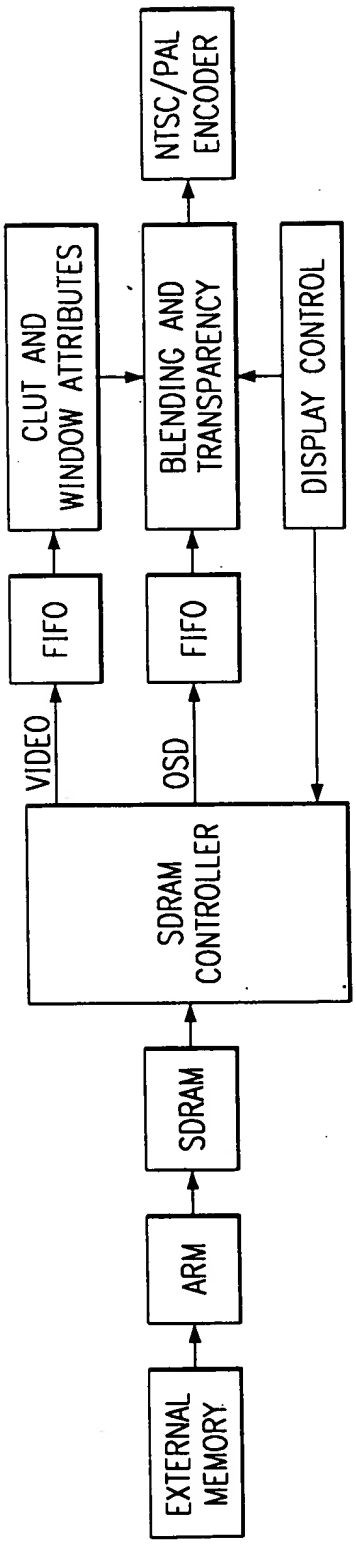

EXTERNAL MEMORY
ARM
SDRAM
SDRAM CONTROLLER
VIDEO
OSD
FIFO
FIFO
CLUT AND WINDOW ATTRIBUTES
BLENDING AND TRANSPARENCY
DISPLAY CONTROL
NTSC/PAL ENCODER

FIG. 15

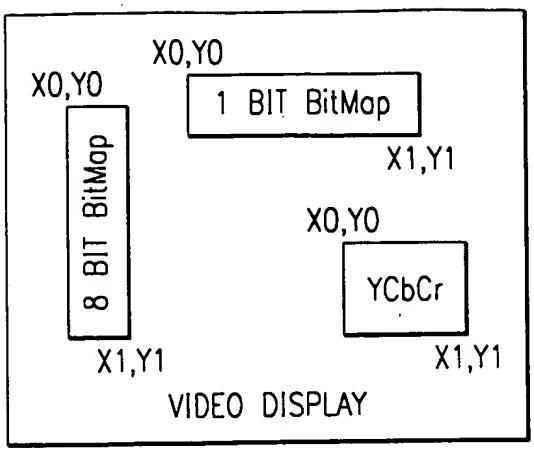


FIG. 16

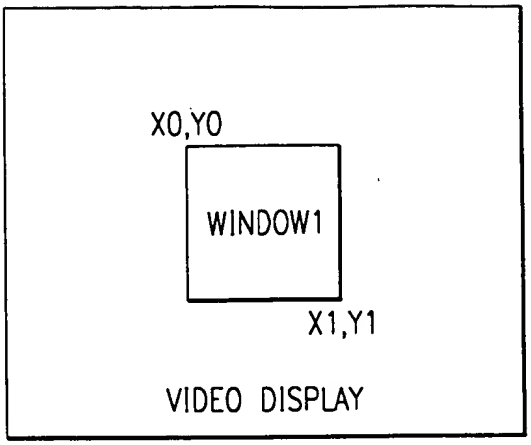


FIG. 17

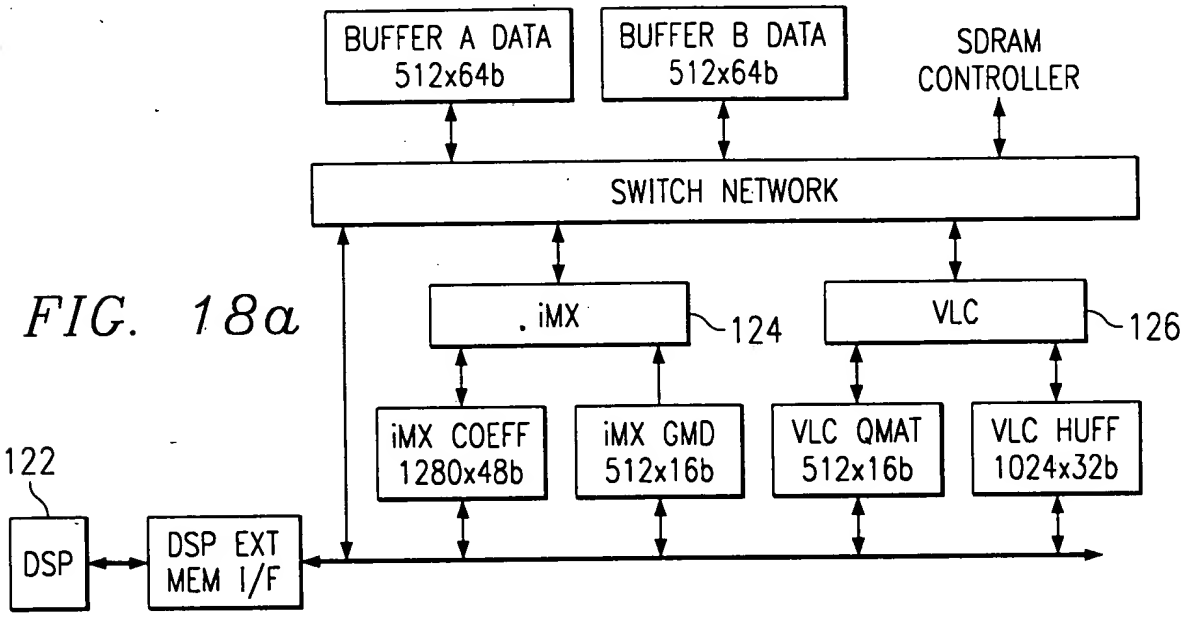


FIG. 18a

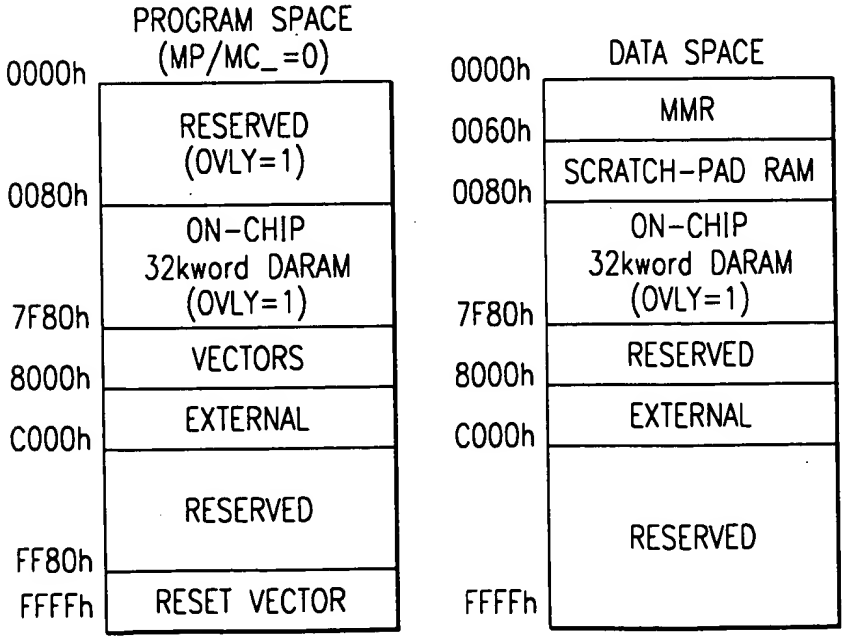


FIG. 18b

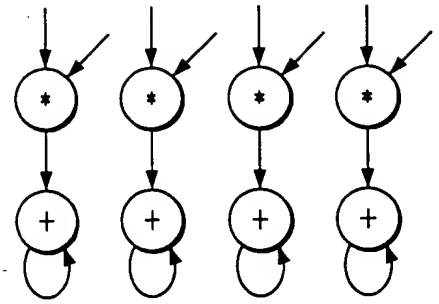


FIG. 19

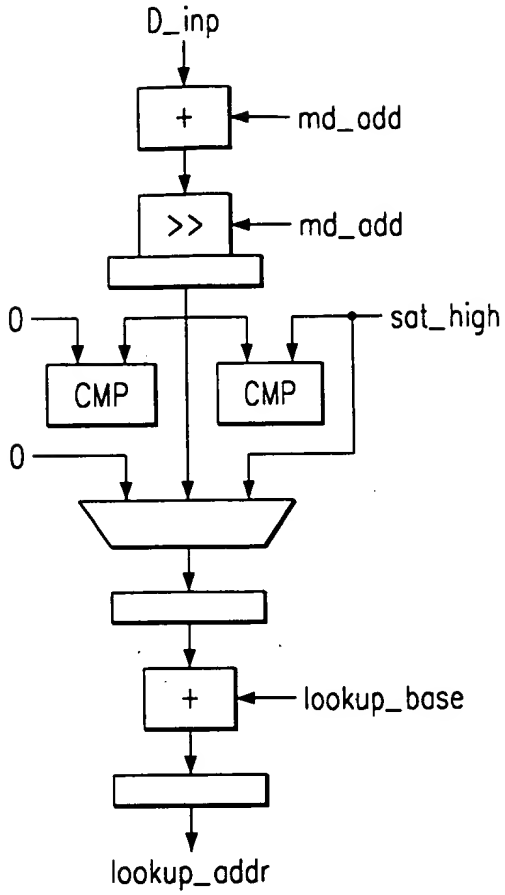


FIG. 21

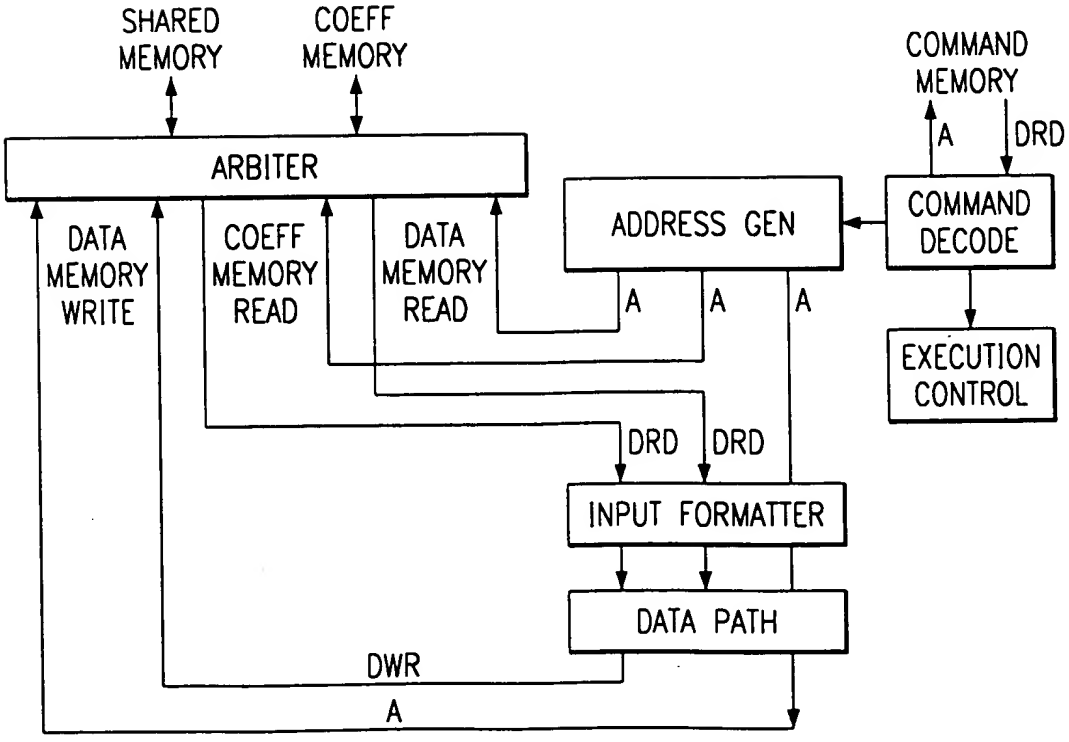


FIG. 20

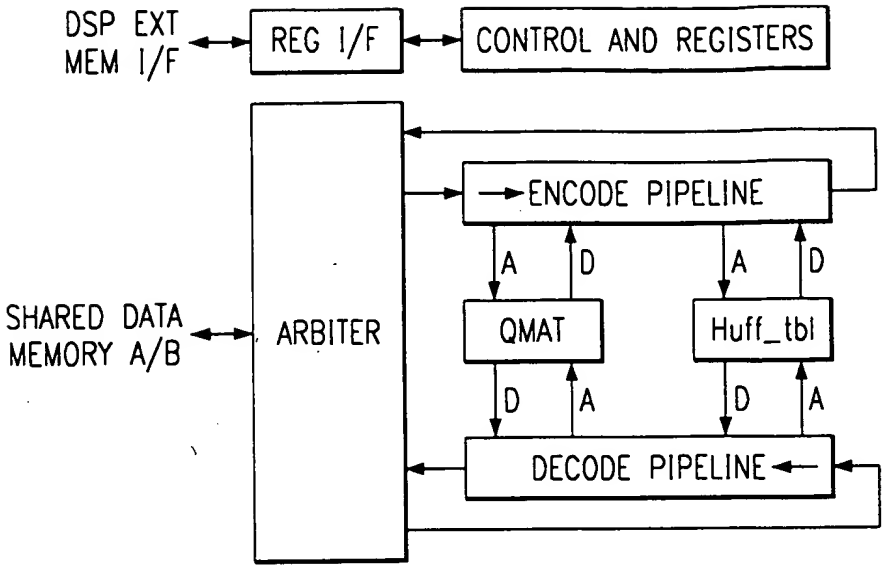


FIG. 22

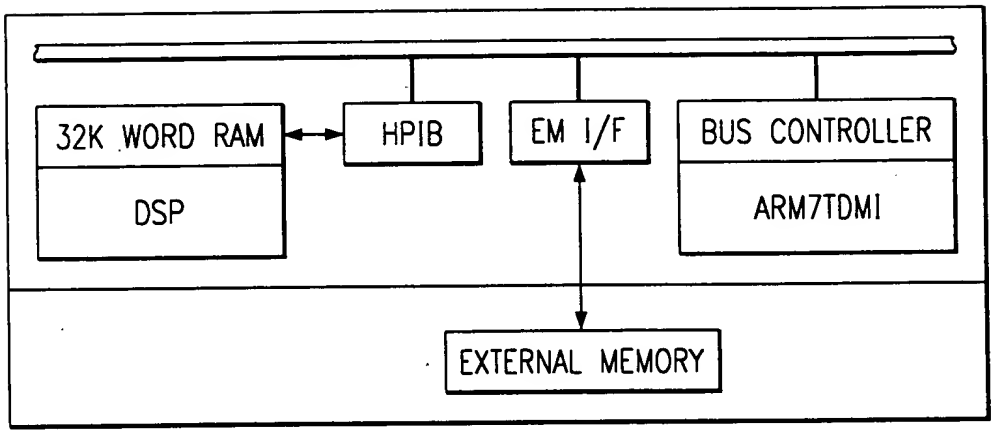


FIG. 23a

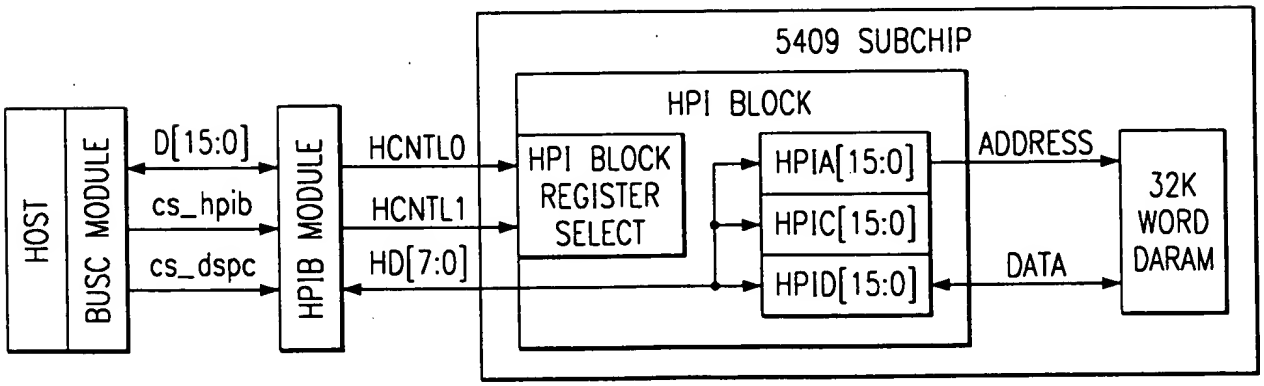


FIG. 23b

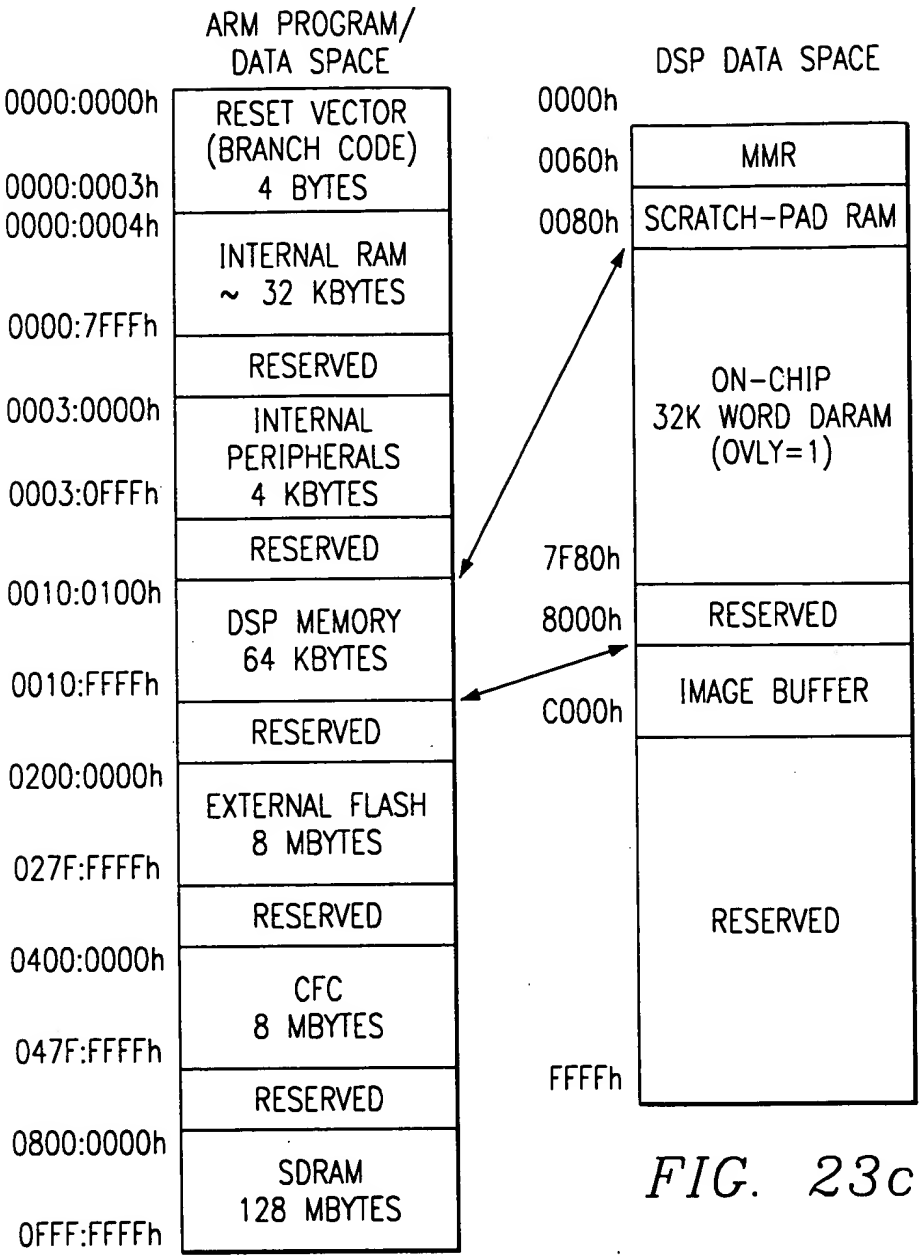


FIG. 23c

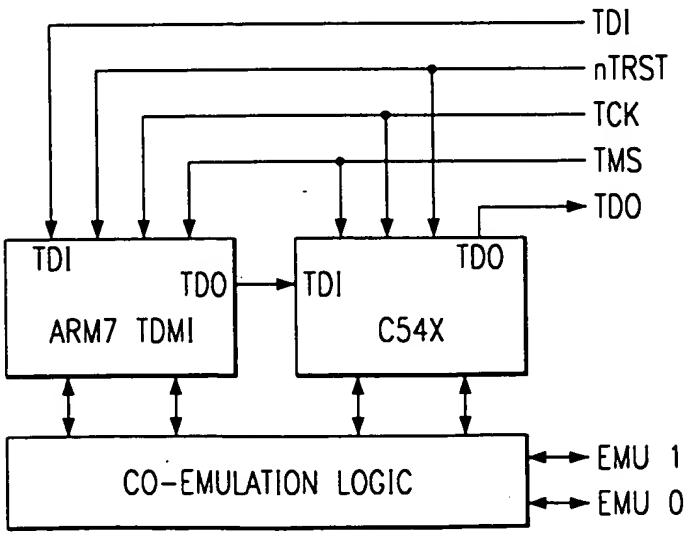


FIG. 24

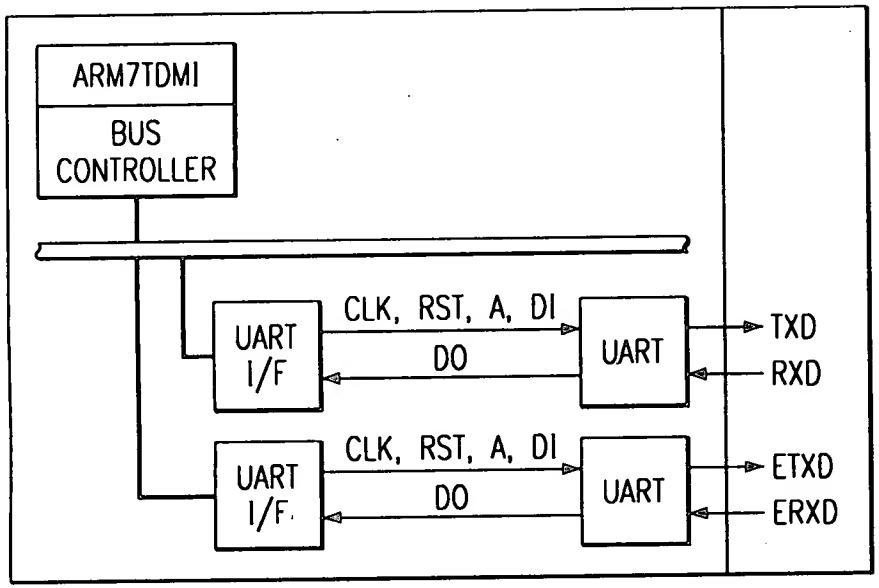


FIG. 25

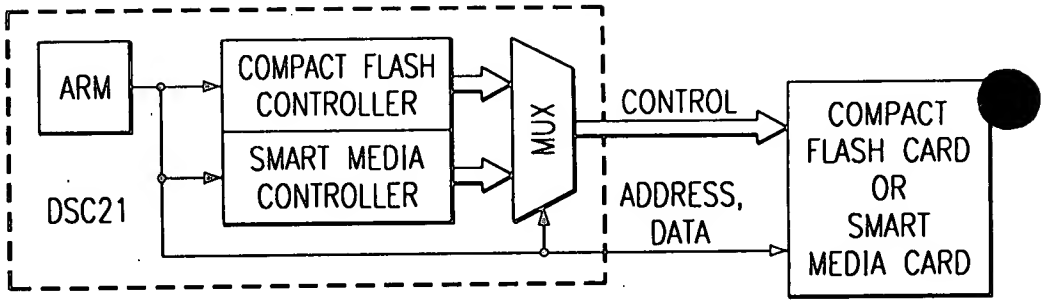


FIG. 26

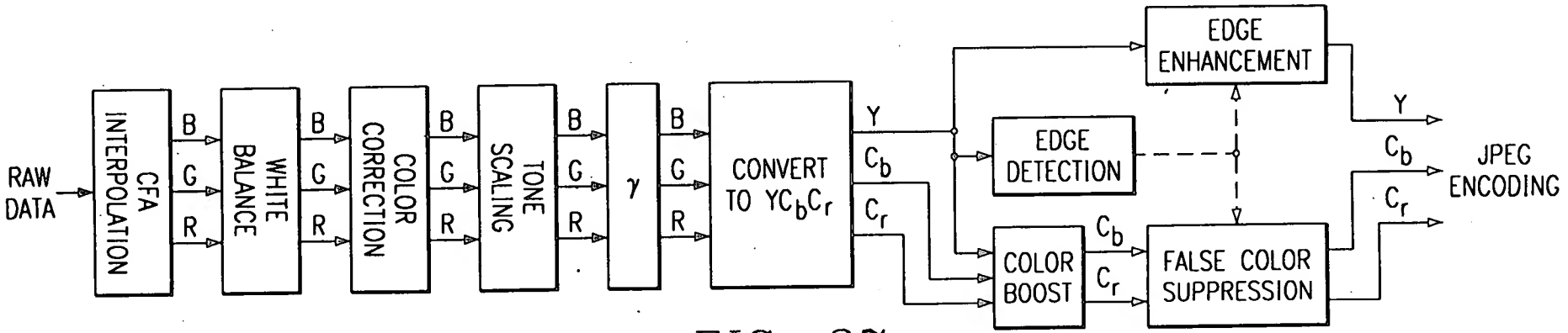


FIG. 27

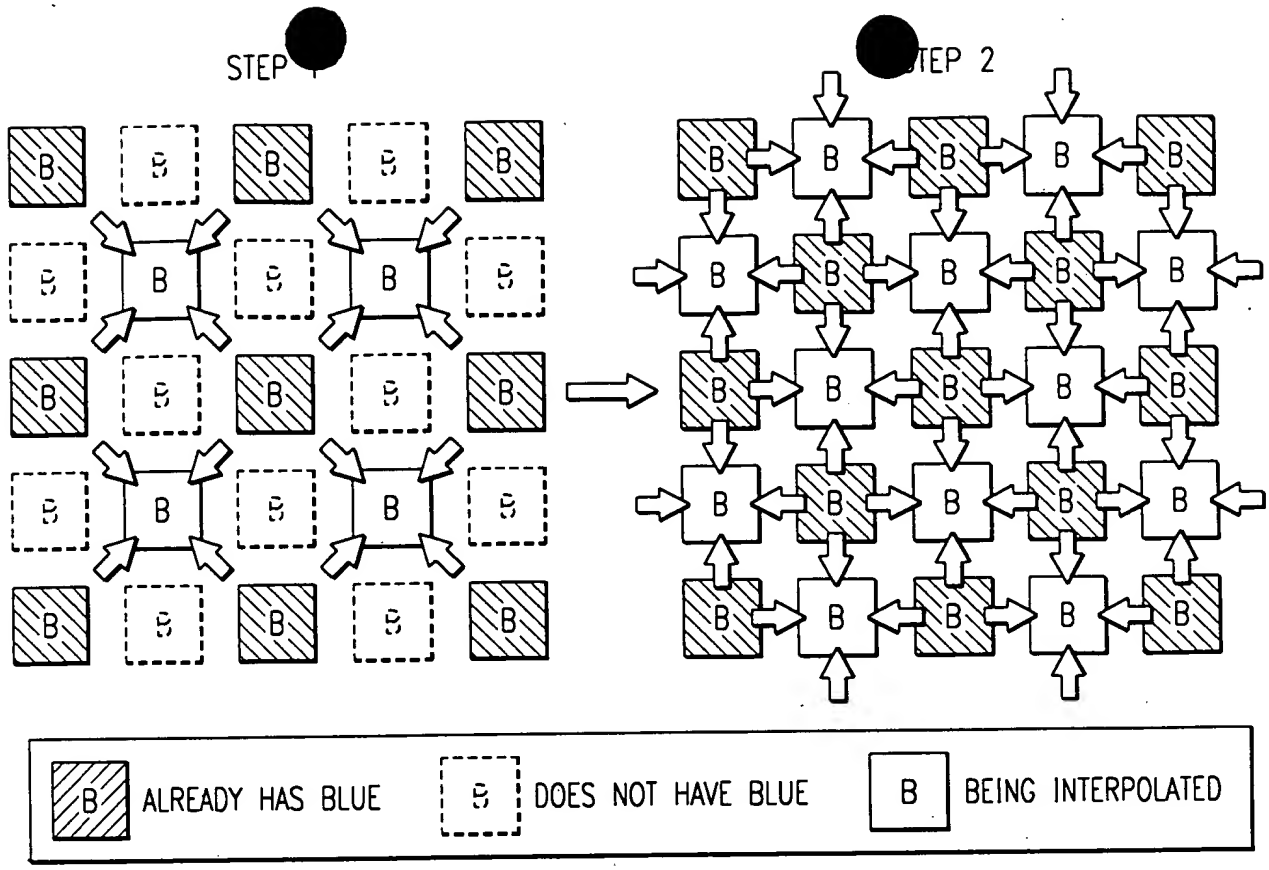

STEP 1
STEP 2
B
ALREADY HAS BLUE
DOES NOT HAVE BLUE
BEING INTERPOLATED

FIG. 28

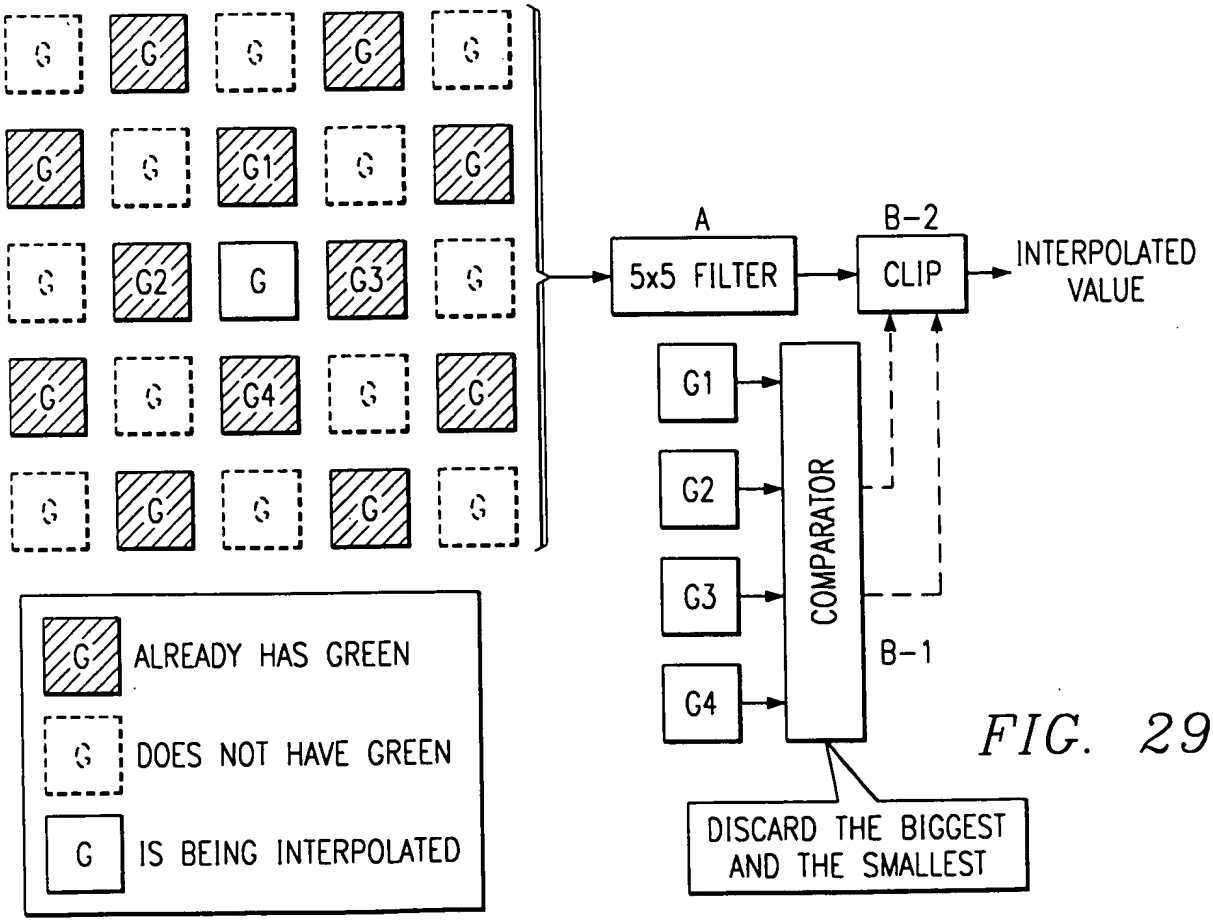

G
G1
G2
G3
G4
A
5x5 FILTER
B-2
CLIP
INTERPOLATED VALUE
COMPARATOR
B-1
DISCARD THE BIGGEST AND THE SMALLEST
ALREADY HAS GREEN
DOES NOT HAVE GREEN
IS BEING INTERPOLATED

FIG. 29

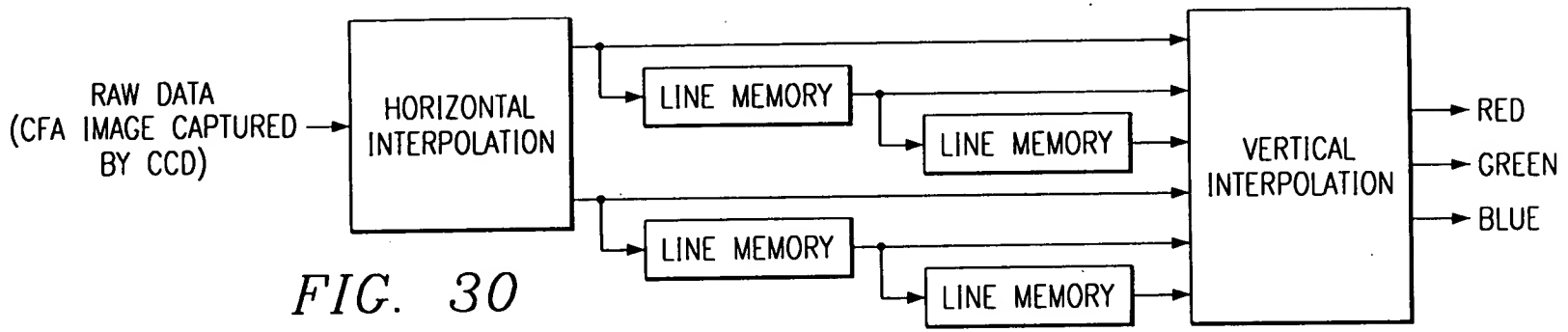


FIG. 30

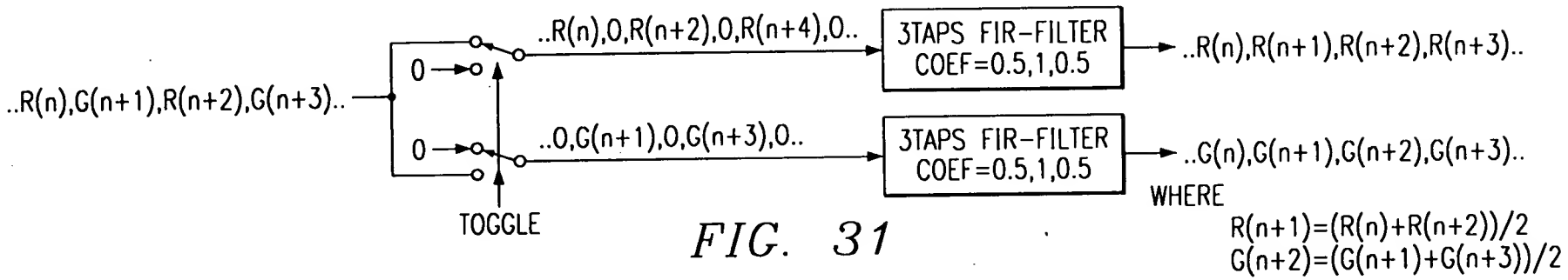


FIG. 31

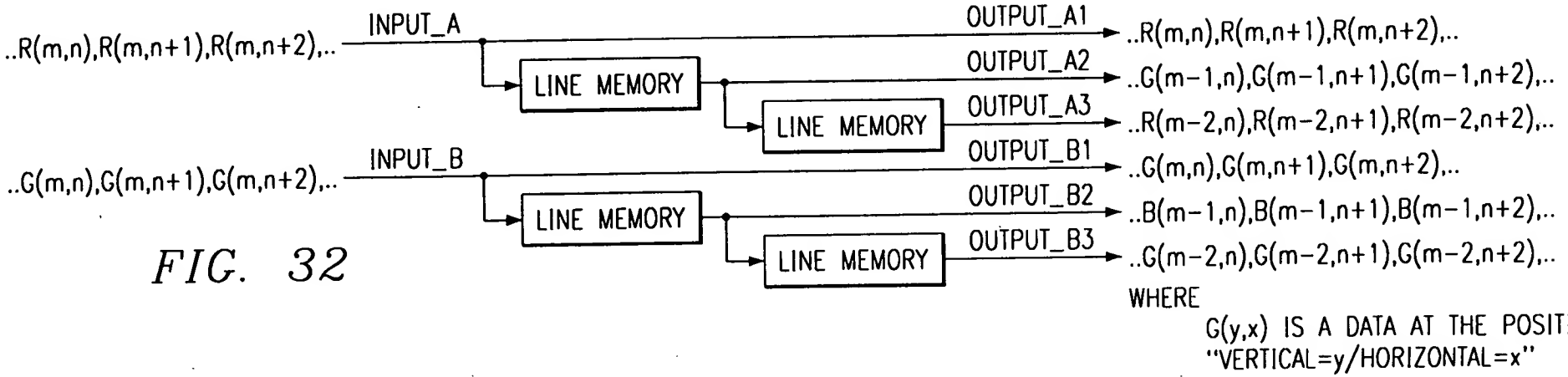


FIG. 32

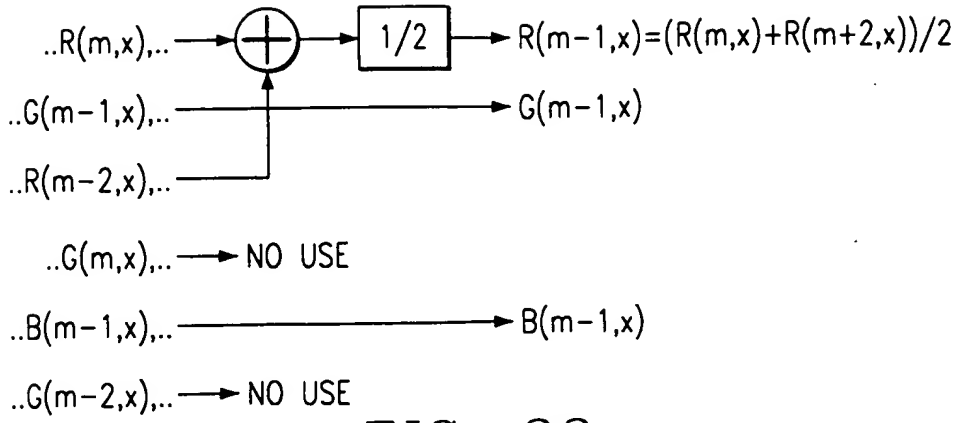


FIG. 33a

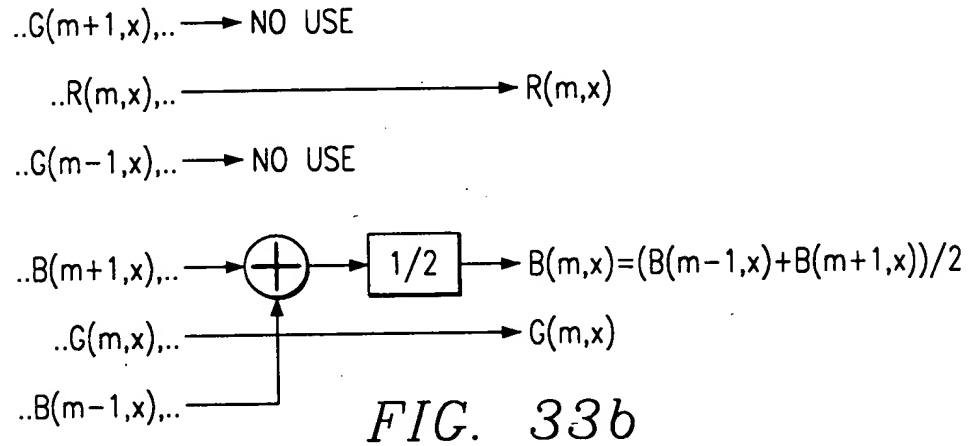


FIG. 33b

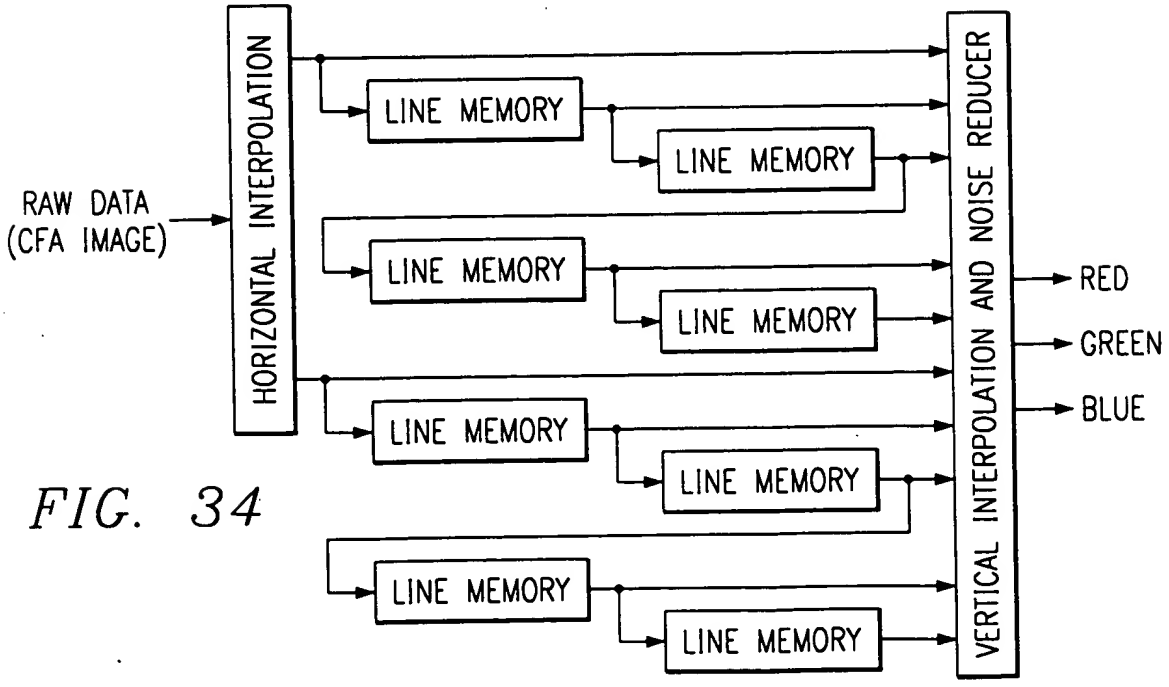


FIG. 34

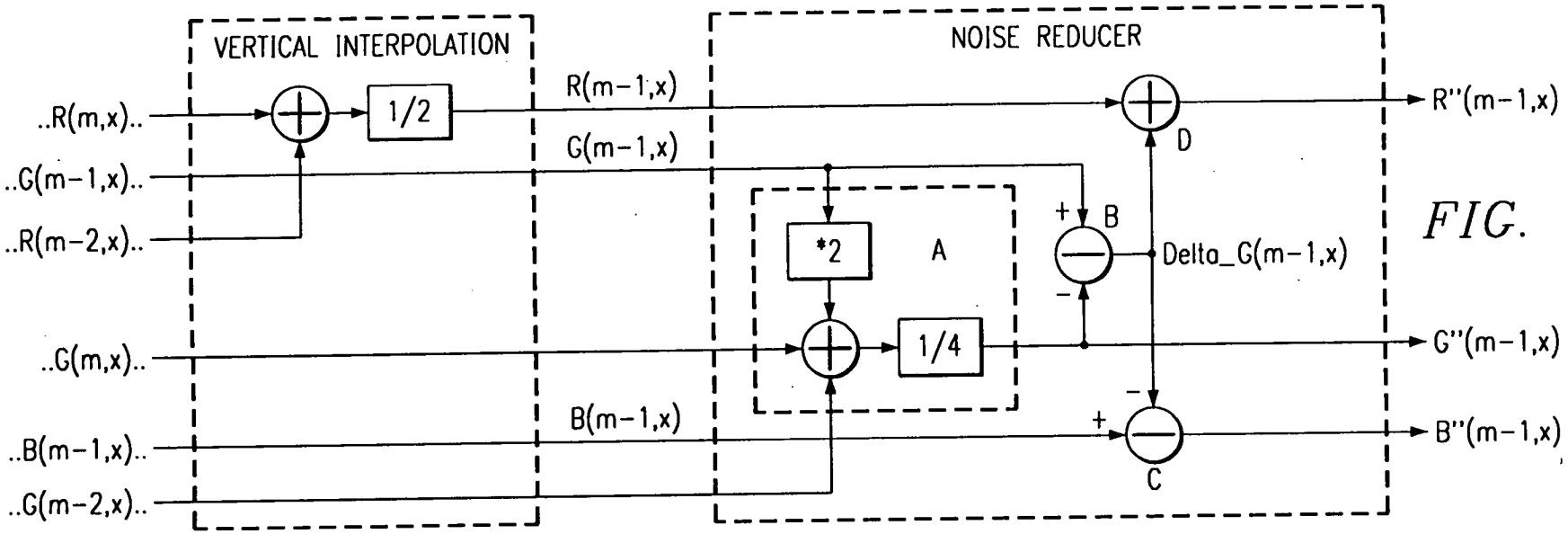


FIG. 35a

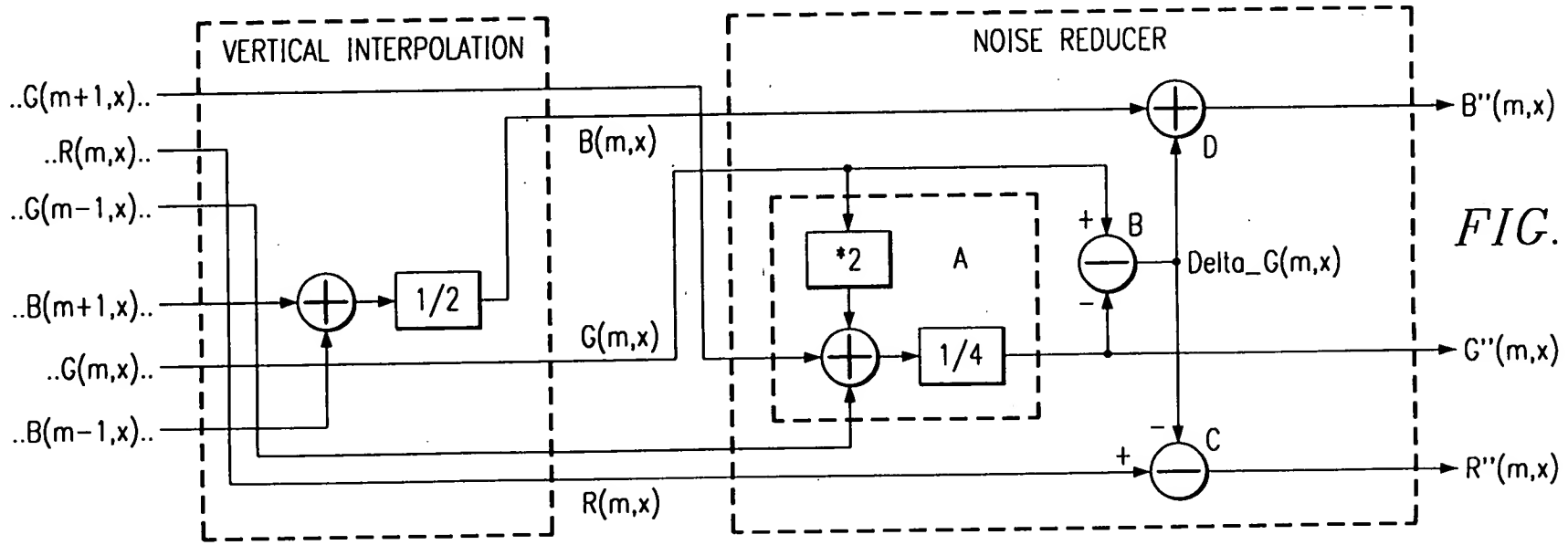


FIG. 35b

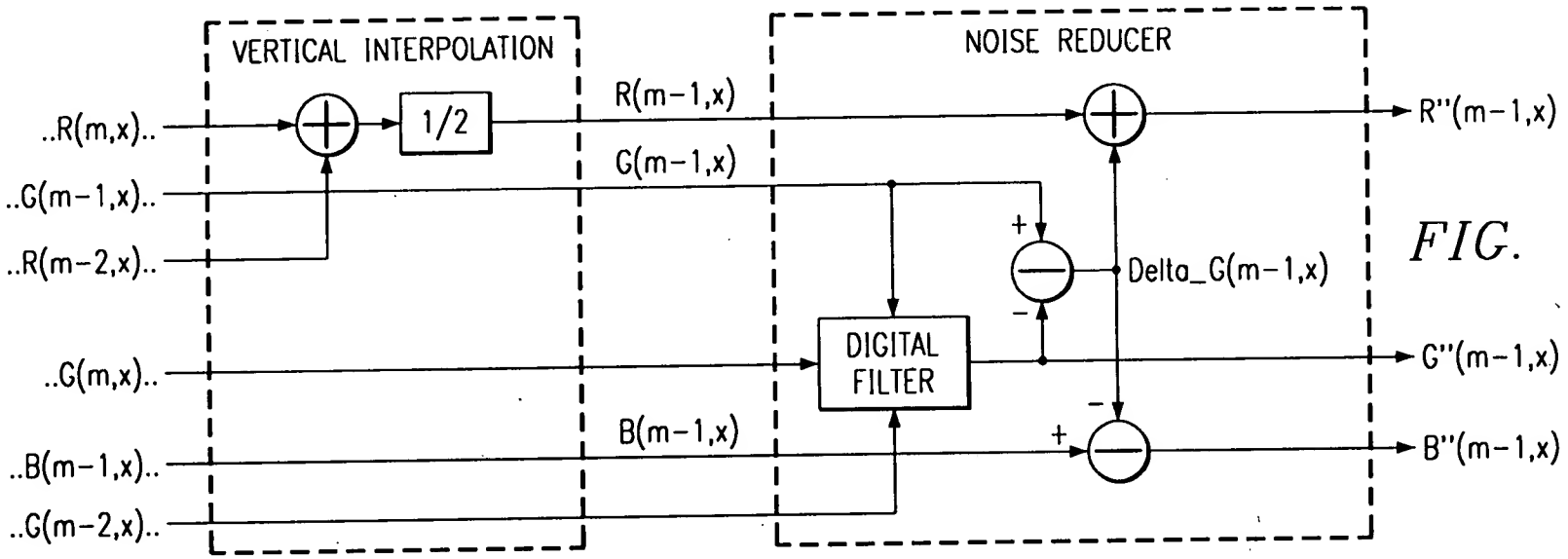


FIG. 36a

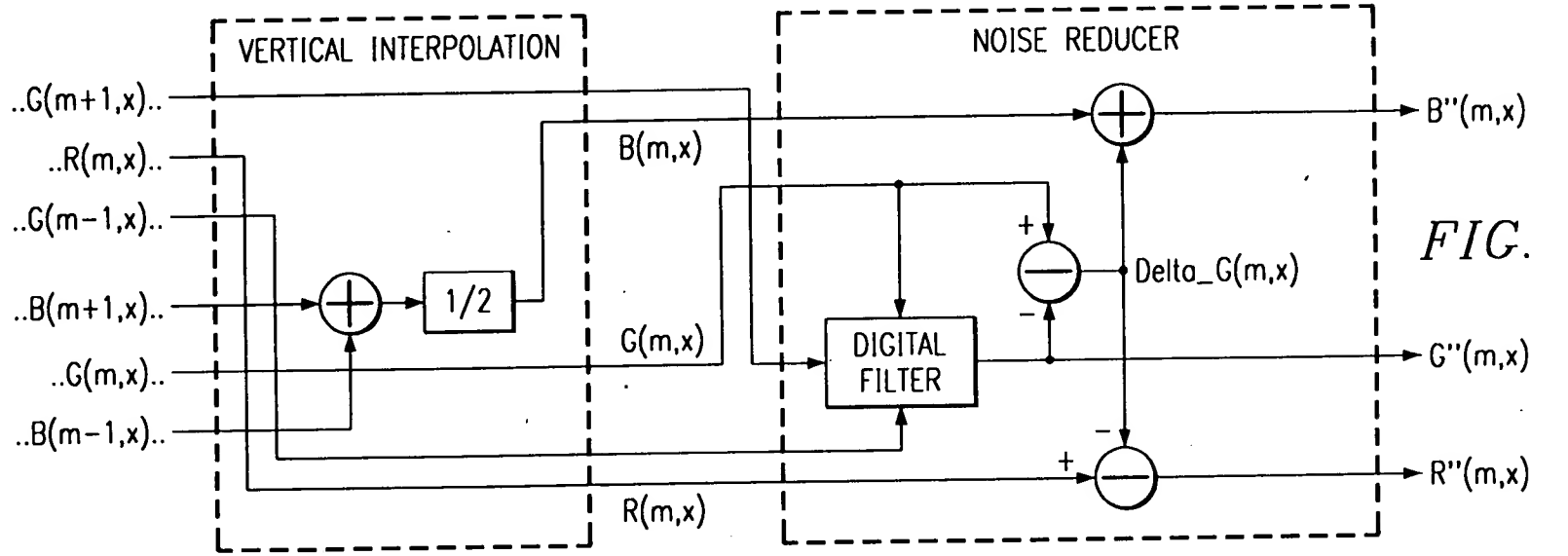


FIG. 36b

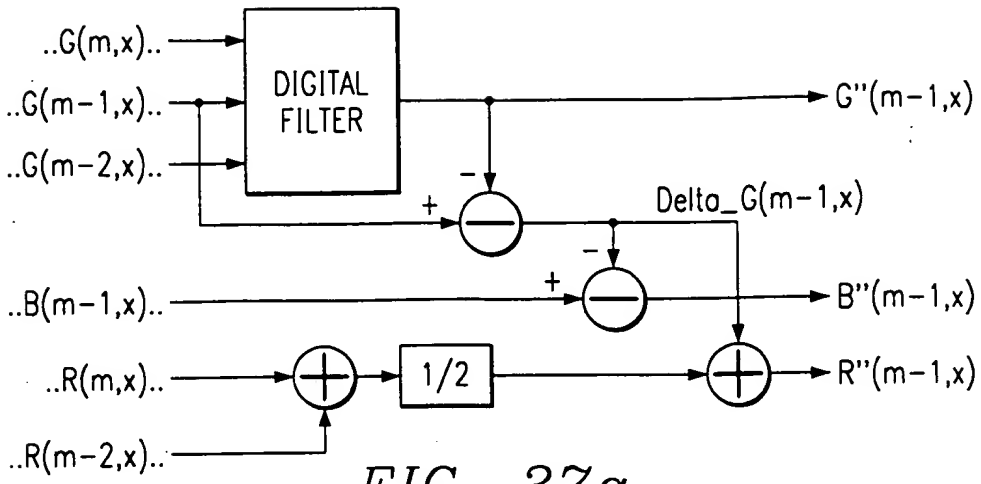


FIG. 37a

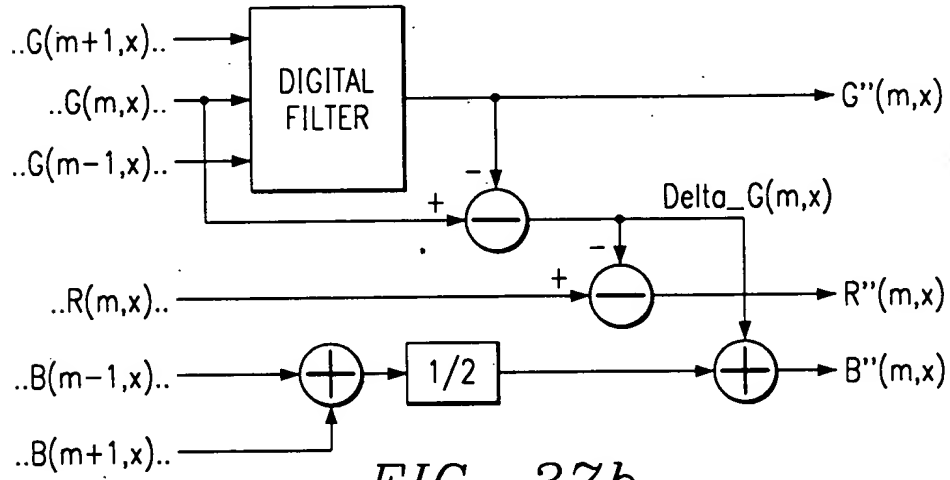


FIG. 37b

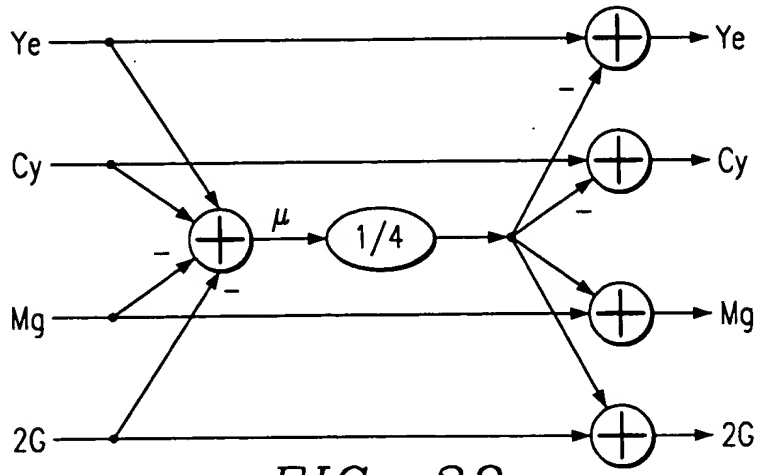


FIG. 38

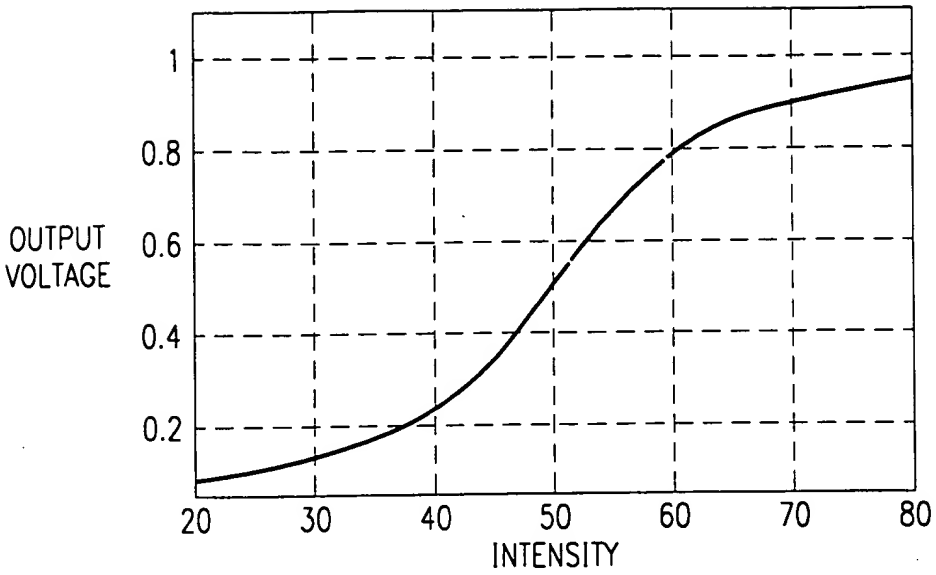


FIG. 39a

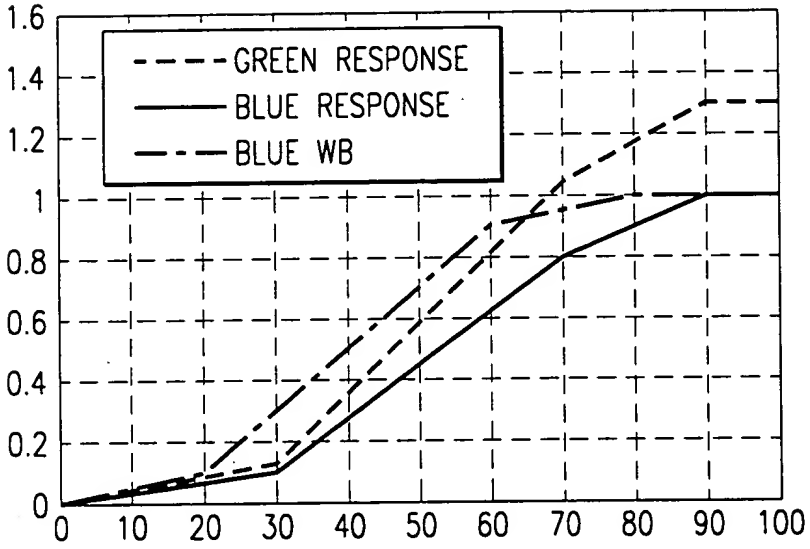


FIG. 39b

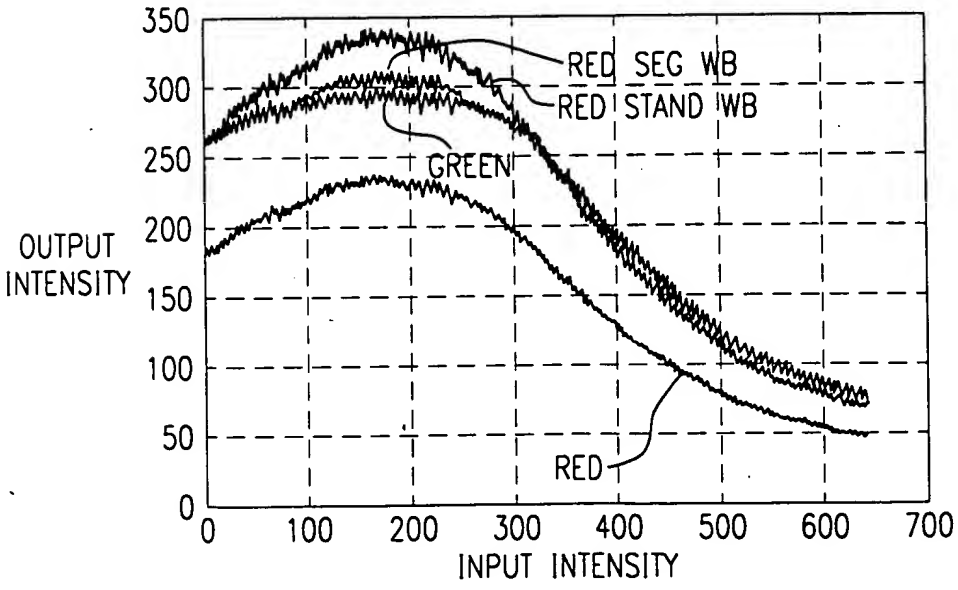


FIG. 40

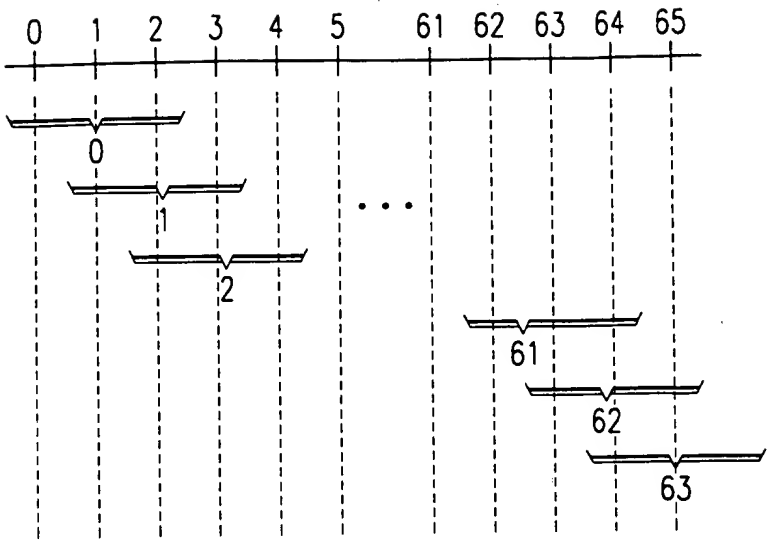


FIG. 41a

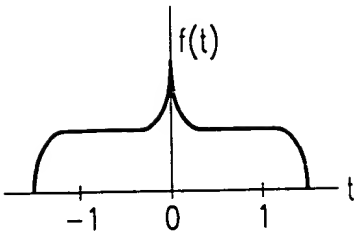


FIG. 41b

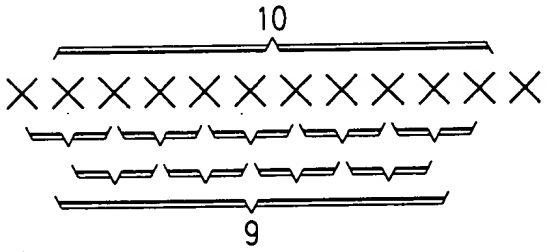


FIG. 42a

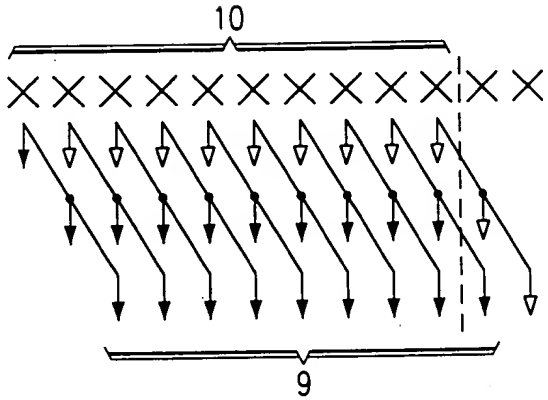


FIG. 42b

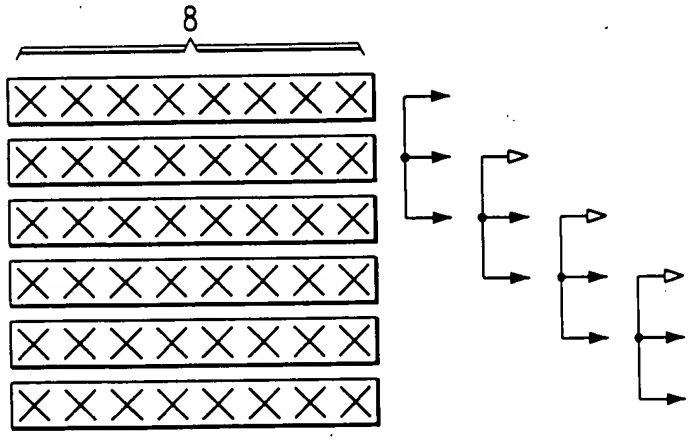


FIG. 42e

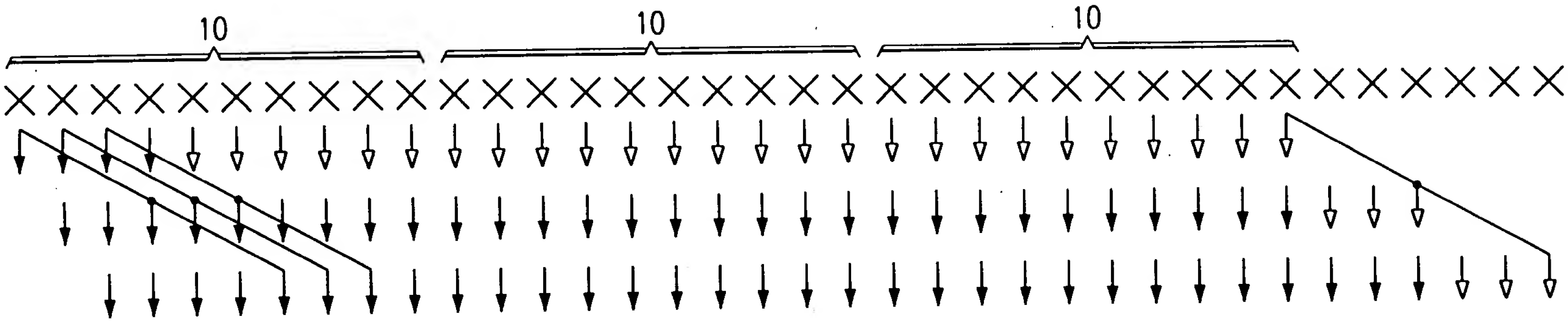


FIG. 42c

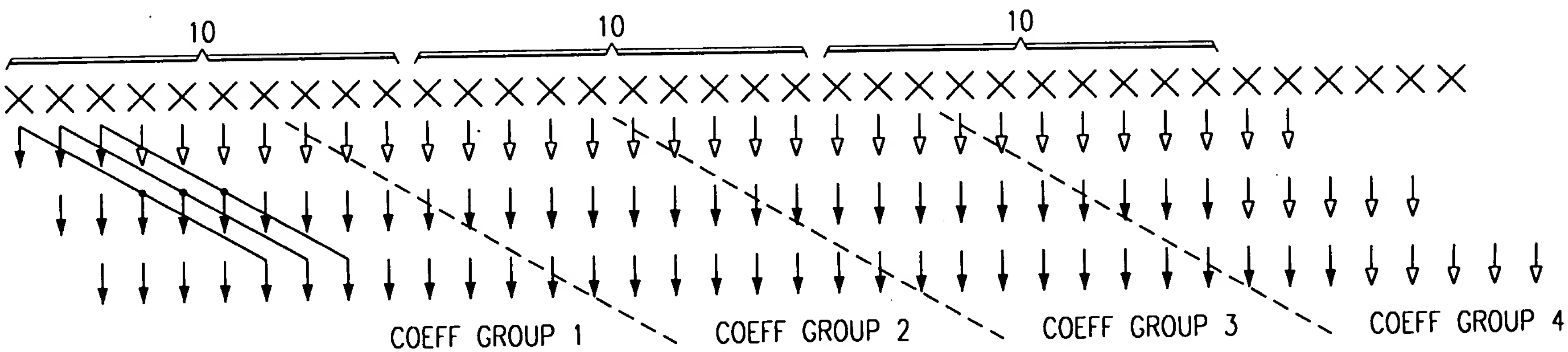


FIG. 42d

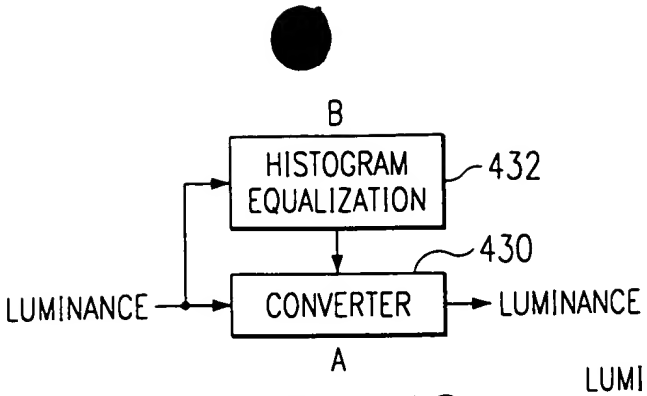


FIG. 43

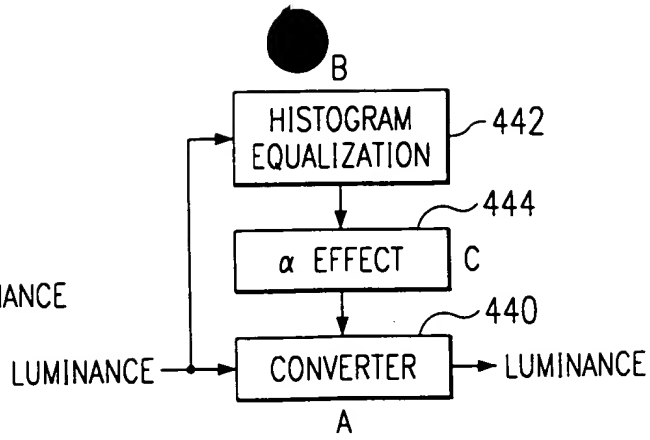


FIG. 44

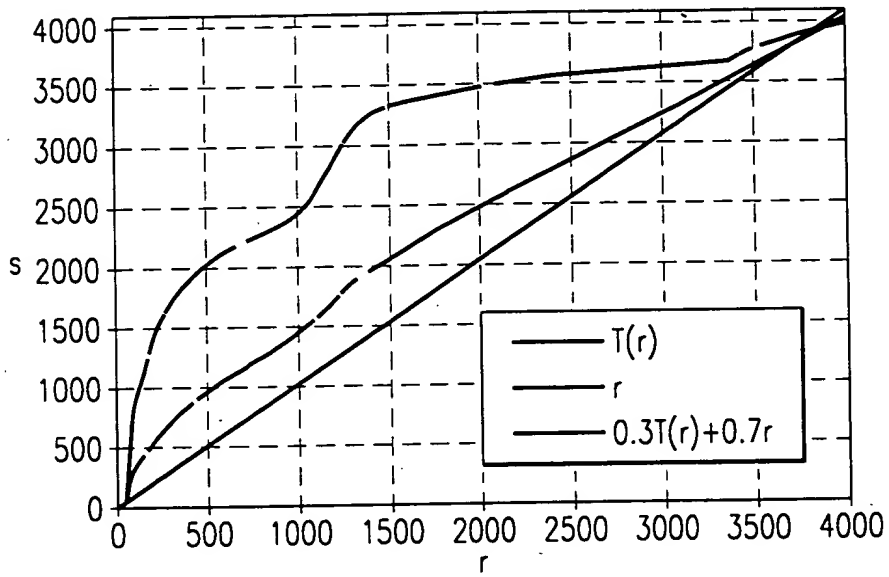


FIG. 45

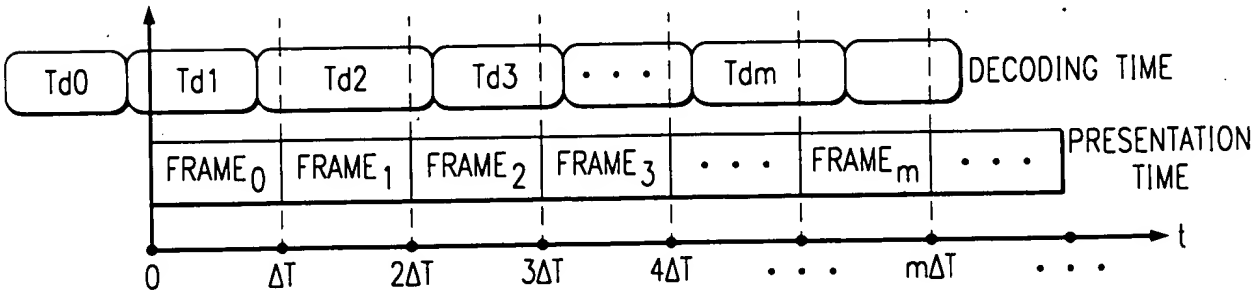


FIG. 46a

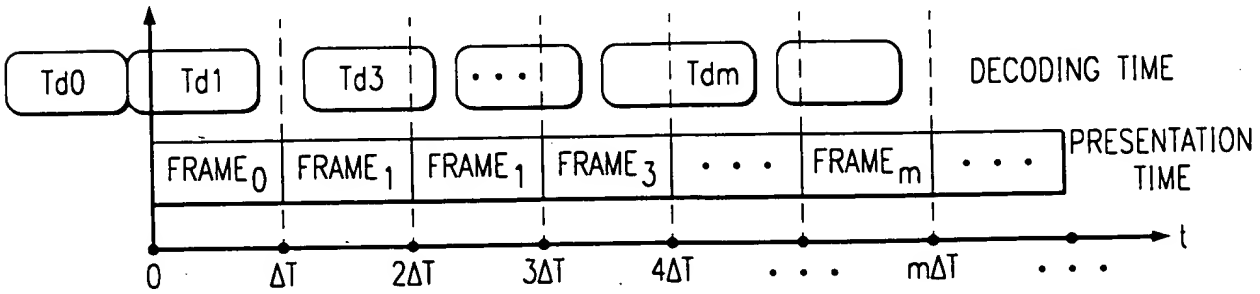


FIG. 46b

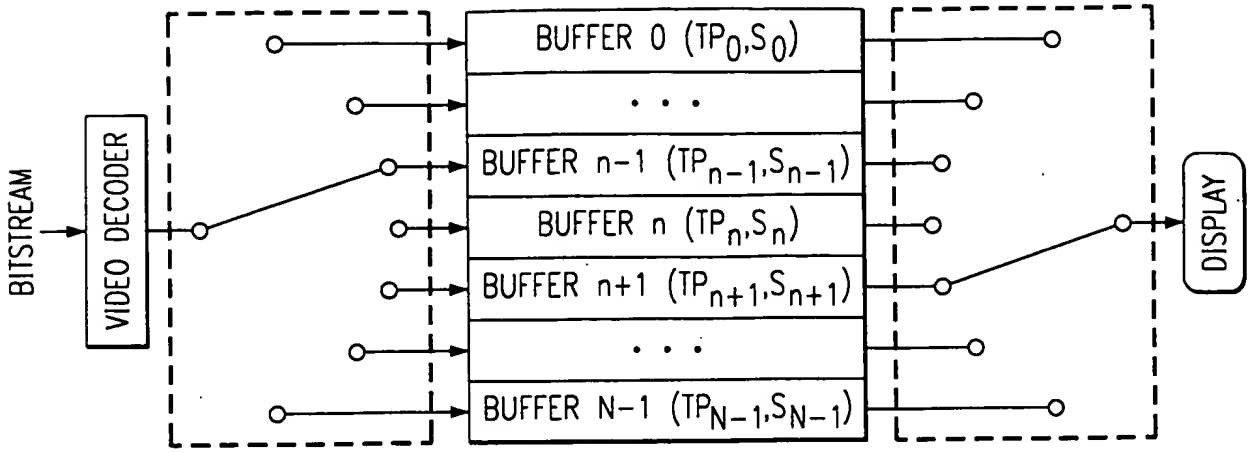


FIG. 47

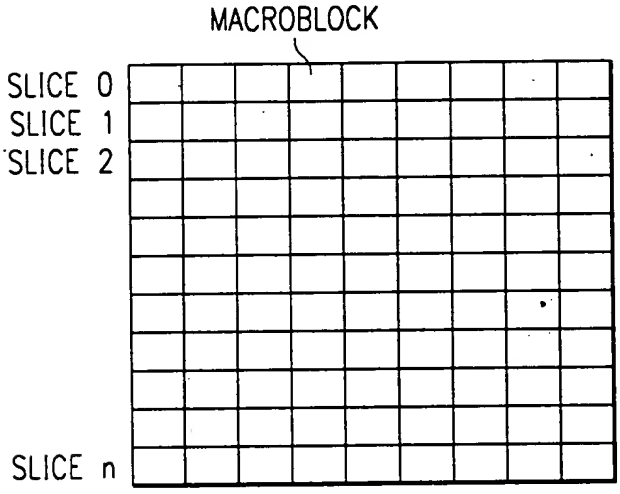


FIG. 49

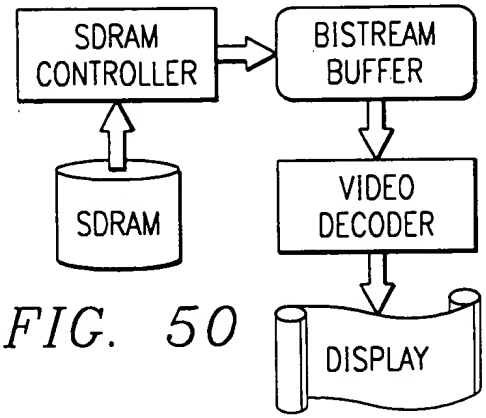


FIG. 50

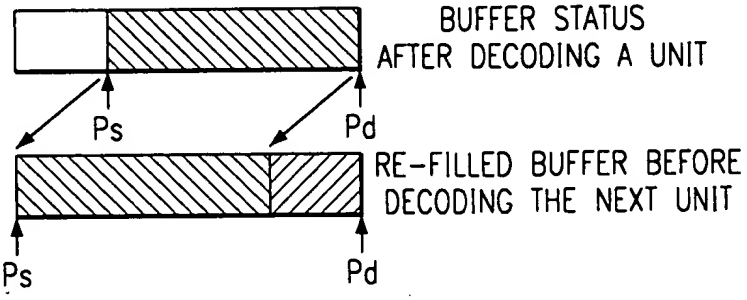


FIG. 51a

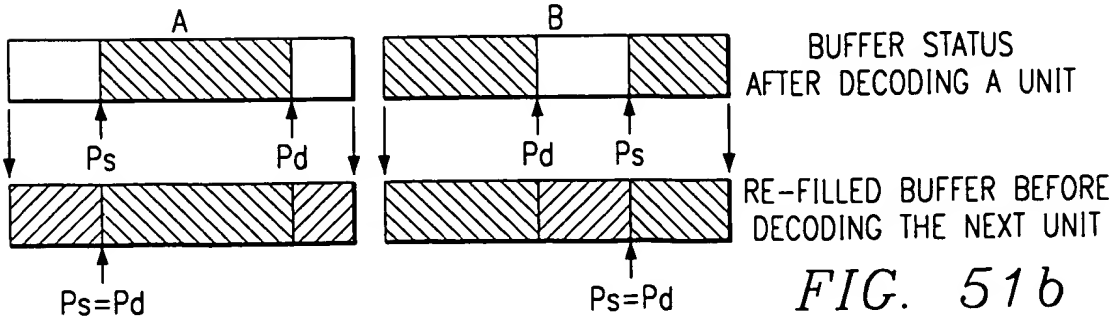


FIG. 51b

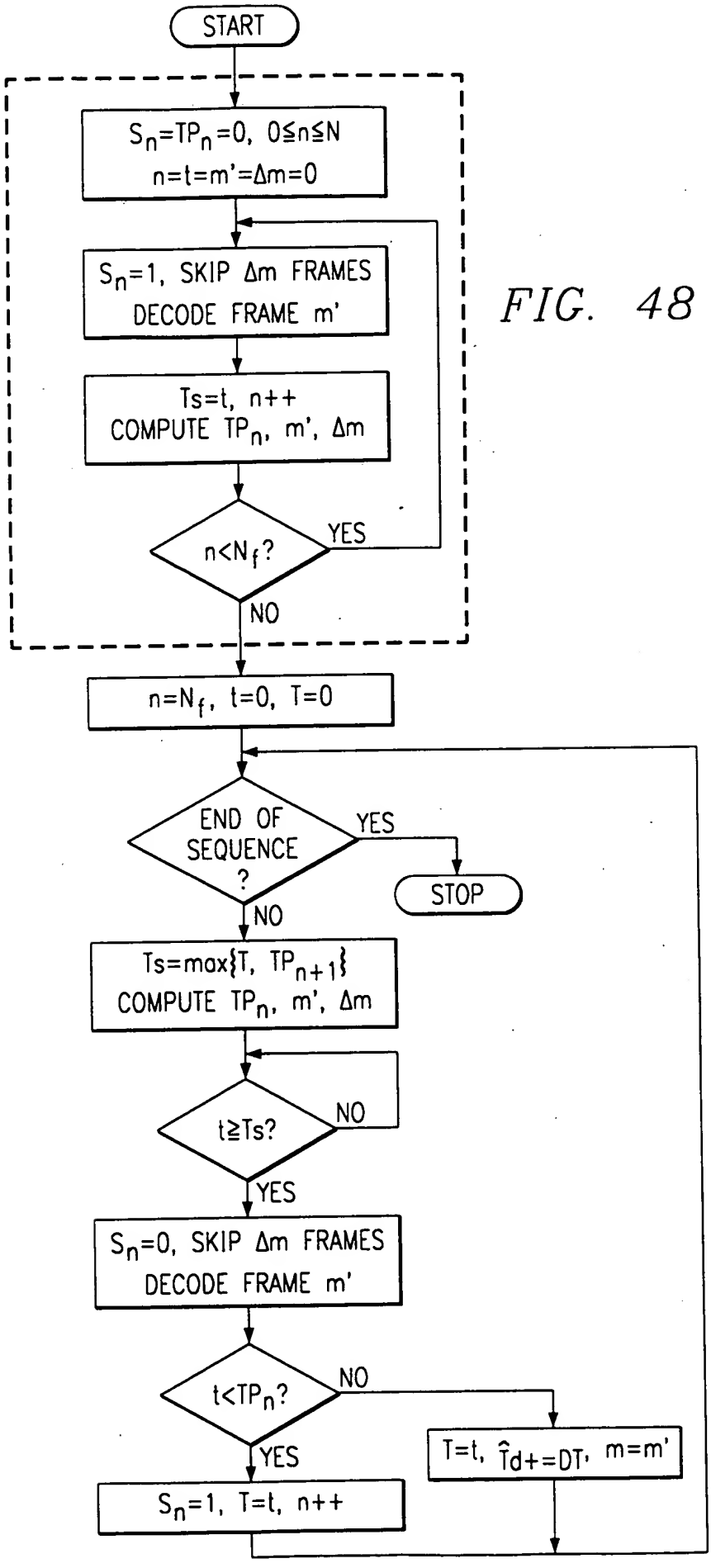

START
$S_n=TP_n=0$, $0 \leq n \leq N$
$n=t=m'=\Delta m=0$
$S_n=1$, SKIP Δm FRAMES
DECODE FRAME m'
Ts=t, n++
COMPUTE TP_n, m', Δm
$n<N_f$?
YES
NO
$n=N_f$, t=0, T=0
END OF SEQUENCE ?
YES
STOP
NO
$Ts=\max\{T, TP_{n+1}\}$
COMPUTE TP_n, m', Δm
$t \geq Ts$?
NO
YES
$S_n=0$, SKIP Δm FRAMES
DECODE FRAME m'
$t<TP_n$?
NO
YES
$S_n=1$, T=t, n++
T=t, $\hat{T}d+=DT$, m=m'

FIG. 48

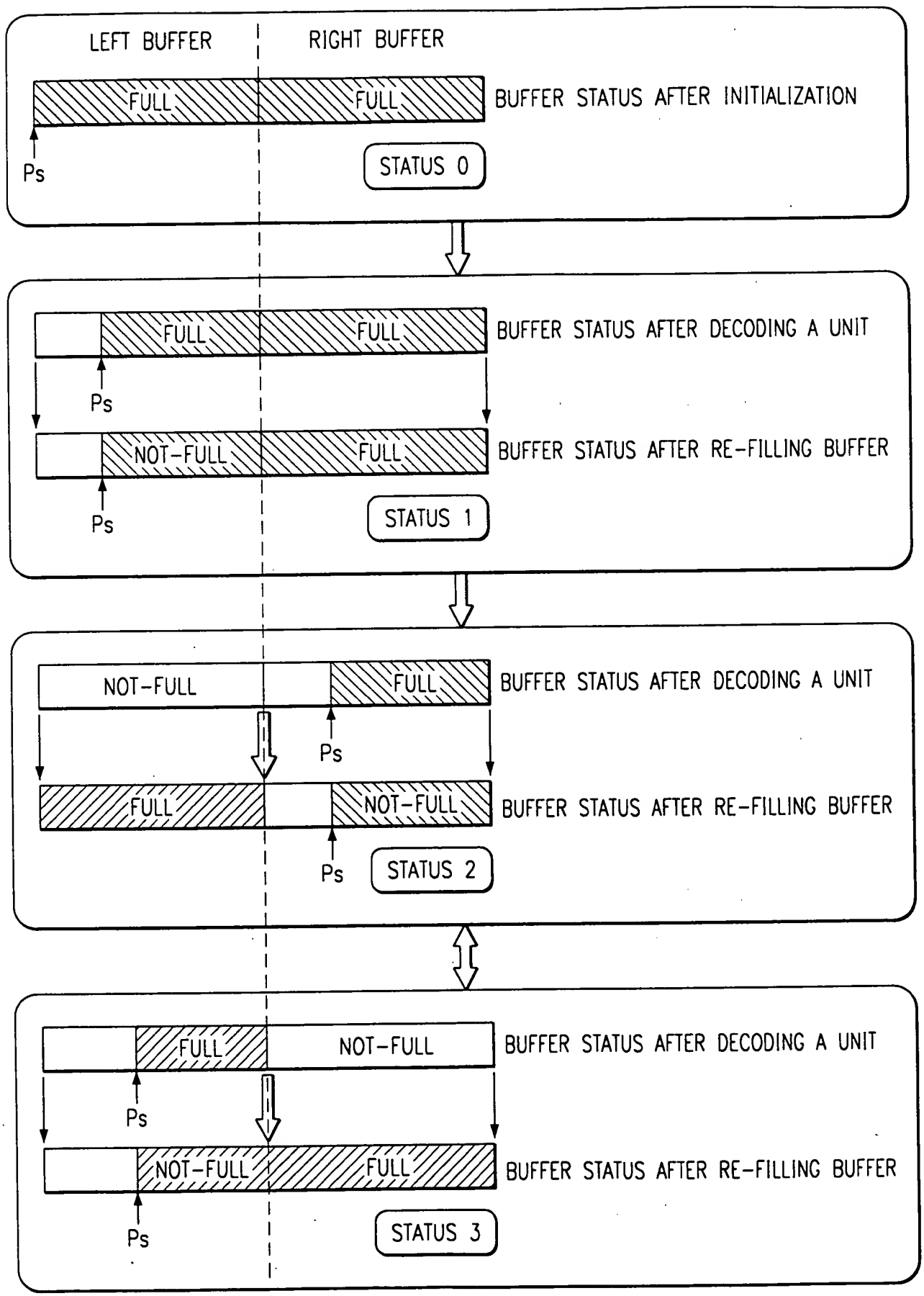

LEFT BUFFER
RIGHT BUFFER
FULL
FULL
BUFFER STATUS AFTER INITIALIZATION
Ps
STATUS 0
FULL
FULL
BUFFER STATUS AFTER DECODING A UNIT
Ps
NOT-FULL
FULL
BUFFER STATUS AFTER RE-FILLING BUFFER
Ps
STATUS 1
NOT-FULL
FULL
BUFFER STATUS AFTER DECODING A UNIT
Ps
FULL
NOT-FULL
BUFFER STATUS AFTER RE-FILLING BUFFER
Ps
STATUS 2
FULL
NOT-FULL
BUFFER STATUS AFTER DECODING A UNIT
Ps
NOT-FULL
FULL
BUFFER STATUS AFTER RE-FILLING BUFFER
Ps
STATUS 3

FIG. 52